Annual report

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Institut für Mikroelektronik- und Mechatronik - Systeme gGmbH

AN - Institut der Technischen Universität Ilmenau

IMMS

INNOVATION

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VISION

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IMMS – Innovative Platform for Industry and Science

In the year 2002, as in previous years, IMMS, the Institute for Microelectronic and Mechatronic Systems has built on its standing as a research and development agency serving SMEs in its own region, Thuringia, and beyond (not only across Germany, but across Europe).
Projects are shared which attract research funding from public sources such as the Thuringia government, the BMBF (the federal German science ministry) or the EU. There are also a number of situations where industry co-operates direct with IMMS without outside funding. All the projects are running successfully and on them about 40 researchers are engaged.

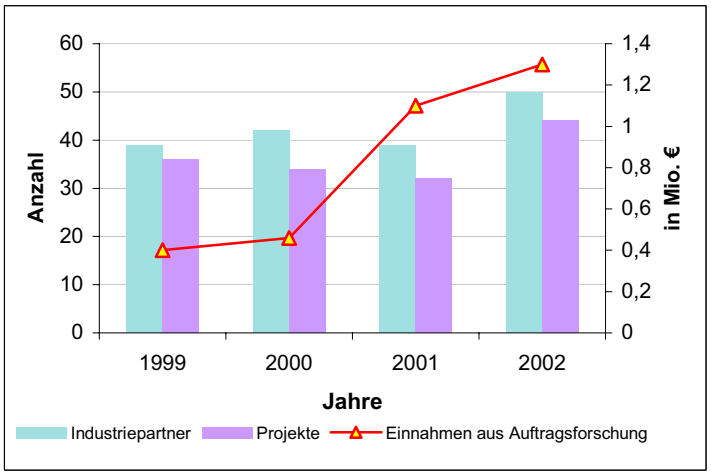

Fig. 1: overview: current receipts of mission oriented research

The division into three departments has proved its usefulness. They have continued in their role, constantly adapting to the demands placed on them by the market in the research areas they cover, which are indicated by their titles, System Design, Micro-Electronics and Mechatronics, and the very much interdisciplinary Circuit and Measurement Technology (see Fig.1).
The work of each department is geared closely to that of the others, so that IMMS can give a complex service to its customers in the design of engineering solutions. The wide range of services at IMMS means that industries of many kinds can be helped with their innovations.
We have customers and research partners from the fields of biomedical and automotive engineering, automation, construction, precision engineering, biotechnology, energy production, equipment manufacture and communications technology.
For our customers, our interdisciplinary teams of experts work out innovative solutions in the course of a detailed dialogue. Our competence in and sensitivity to the potential applications for micro-technology, continue to enable us to push back the horizons, affording our customers to open up their markets with product development and diversification.
The fact that some of IMMS' former employees have themselves set up in business and industrial use of our research outcomes has had a valuable multiplication effect. These companies are themselves providing high-tech jobs for Thuringia.

Particular effort is at present being applied to the winning and keeping of R and D partners from Germany and abroad, and likewise partner enterprises, for a variety of longer-term projects (see Fig. 2). For instance, it was possible in 2002 to tackle certain new European projects, combining pure research into industrial precision drives (including investigations of relevant materials to pair up under different operating conditions such as ultra-high vacuum) with research into the speeding up of design engineering where micro-electronic circuits are concerned. The aim is to produce analogue and mixed signal on-chip circuitry.
The joint projects with various departments of our local university, the Technische Universität Ilmenau, continued and new ones were begun.

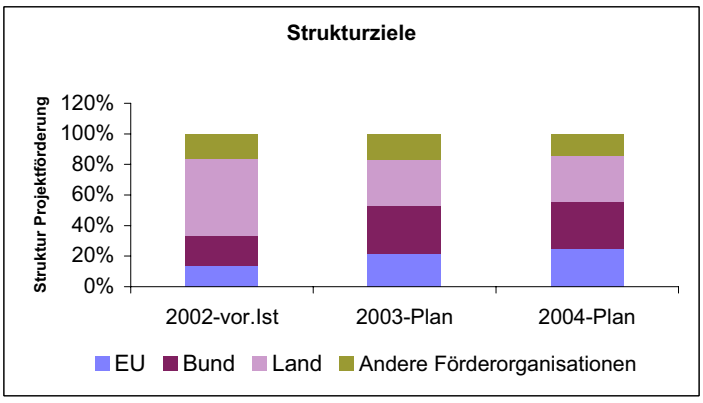

Fig. 2: Industrial partners by provenance

Pure research funded by the DFG (German Research Council) is taking place and IMMS also has a share in the newly established Special Research Project 622 called "Positioning and Measurement Machinery in the Nanometre Range".

Being an associated institute of the Technische Universität (TU), IMMS provides many students and academics with work on either a paid or a placement basis, with the opportunity in many cases to write undergraduate papers or dissertations for the German Diplom and for doctorates.
The TU has such newly founded or established institutes as the APC, or Applications Centre, and the ZMN, Centre for Micro- and Nanotechnology. With them, IMMS is involved in an increasing number of co-operative contracts.
The year 2002 saw the reaching of a significant milestone when the Erfurt branch of IMMS moved into new premises at the AZM in south-east Erfurt – the abbreviation stands for the German name, which translates to "microsystems engineering application centre". There, 15 members of staff are pursuing their activities in that field, with plenty of space to work in: about 330m². The intention is to increase the number of staff to 25 and make use of the special laboratory facilities to provide measurement technology in support of opto-electronic and high-temperature circuits. The facilities will also enable the staff to work on analogue integrated circuits for extremely high frequencies and ultra-high precision.
In April 2004, when it is hoped that the new Ernst-Abbe-Zentrum für Forschung und Transfer on the TU campus will be finished, IMMS is contracted to move into the new centre. The contract for rental and use was signed in November 2002 with the trustees of the Ernst-Abbe-Stiftung (Fund) of Jena, who have financed the new research centre with its facilities for transfer of academic results to industry. The plans for the final shape to be taken by IMMS, integrating it into an up-to-date infrastructure, are thus in place and should reach fulfilment by the end of the year 2006.
The present report again presents the core areas of competence of the institute and the R and D outcomes therein achieved. It is, at the same time, to be read as an offer of further services if these are sought by potential new partners within Germany and abroad.
As has been the case since the institute was founded for this purpose, our range of subjects is wide and we are a strong research partner supporting the development of small and medium-sized enterprises in (particularly) Thuringia. What IMMS can offer is

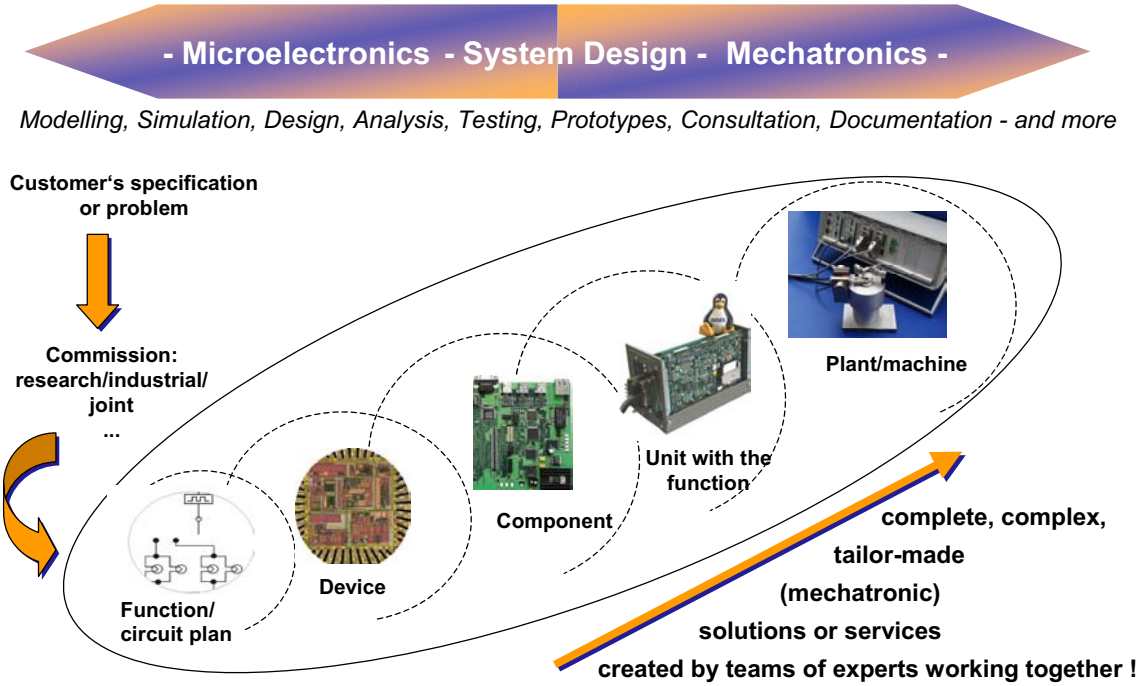

Fig. 3: Services provided by IMMS

- an innovative platform where industry can develop in partnership with us exploitable skills; in other words, strategic underpinning of Thüringen's technological business plans
- a gateway to new marketing potential for our clients, giving them the leading edge in their field. IMMS is a driving force that sets new technological landmarks for industry.

- staff development, for in their skills and creativity, the IMMS researchers are not only the human resources of the institute, they are the greatest factor in its success.
- opportunities for the staff to consider moving into business in their own account with the assistance of IMMS, so that development is converted to industrial use within a network of trusted partnerships.

It is the IMMS strategy to concentrate on

- being an integral part of relevant groups and networks so that what it does best will benefit Thuringia companies and their marketing needs,
- providing a centre of excellence organised around the disciplines of system design, microelectronics and mechatronics (see Fig. 3),
- taking part in co-operative projects at national and European level with funding from the German government and the EU

The managers of IMMS would like to acknowledge the contribution of all our industrial, academic and political partners, the trustees of the funds on which our institute depends, the members of our board of directors and our academic council. The mutual trust experienced our joint work with them is much appreciated. To our staff, above all, we also express our appreciation, for their commitment, creativity and sheer hard work.

Ilmenau, January 2003

Professor Gerd Scarbata
Exec. Director, Research

Hans-Joachim Kelm
Exec. Director,
Administration

Mechatronics

Aims

In the Mechatronics Department, precision drive systems are designed, analysed and tested for the most varied fields of application. The work involves not only design and construction but also optimisation. This last is achieved by modelling and simulation of the heterogeneous systems, which are in some cases extremely complex. The modelling permits accurate and dependable predictions of the systems' behaviour, for example in respect of mechanical deformation, dynamics, and magnetic or thermal behaviour, so that the number of design cycles is reduced to a minimum. The tools used for the purpose include Ansys, Maxwell and Matlab/Simulink. Design and construction is supported by Mechanical-Desktop, Inventor or Pro/Engineer.
The subjects addressed by the Mechatronics Department -

- direct drive systems
- analytical tools and equipment
- drives for use in UHV and
- complex mechatronic systems

are subjects which overlap even within the Department of Mechatronics on the one hand, and, on the other, link closely to the fields of System Design and Smart Power Systems.
Our approach in project work is, above all, to take a holistic view of the system and its optimisation. Close interdisciplinary co-operation between experts combined into project teams and staff from the commissioning company is always the pattern.

Special fields of application

To take some examples, drives that have been designed at IMMS have the following characteristics, :

- high accuracy and excellent dynamics even in multi-track movement (in the case of multi-axial direct drives)
- the use and combination of a variety of physical movement principles (e.g. electrodynamic, electromagnetic or piezo-electric).
- control by means of systems with innovative strategies.

We find tailor-made drive solutions or applications and adapt them with suitable sensors and control systems for integration into plant and equipment. We also command considerable knowledge on which to base the design of plant by combining conventional drive, sensor and control components.
Measurement and control systems are available in plenty to help us assess and optimise the drive properties and to carry out rapid prototyping when designing the best regulatory software.
We have developed or are still in process of developing and investigating:

- a drive system for a 3-D precision gauge (p. 10)
- the PMS100-3 high-precision positioning system (p. 11)
- planar drive systems for microsystems engineering (p. 12)
- an online-capable rheometer (p. 13)
- a control system for high-precision linear and planar hybrid step drives (p. 14)
- 5-axis positioning systems for high-precision polishing of fine optical components (p. 8)
- planar electrodynamic direct drive systems
- devices and instruments for analytical purposes (e.g. microtribometers)
- design of digital regulating systems with multiple axes.

Tasks we envisage for the future are:

- design and implementation of track control systems for multiple-axis drives
- drives for wafer positioning systems
- optical surface measurement technology
- positioning systems for the nanometer range and wide fields of movement.

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Design, construction and control of a positioning system with 5 axes

Objective

A development project has been run jointly in Ilmenau by the FSU (Friedrich Schiller University), Jena, and IMMS on the production of a 5-axis positioning system for the polishing of optical components.
Research into the machinery already available on the market led to the conclusion that a completely new design was needed to meet the special demands of the polished optical component trade.
IMMS had in earlier years already gathered a huge amount of experience in developing drives and positioning systems, especially those with direct drives and air-bearings. The experience had included mastering many mechanical aspects of design and developing much know-how on the relevant control systems.
The maximum distances specified for the travel of the polishing tool were 400mm, 160mm and 200 mm in the *x, y* and *z* directions. The positioning accuracy needed to be within 2 µm. There was also a need to provide for tilting round the *x* and *y* axes by 5°, with accuracy of this angle down to ≈ 4 “.
The polishing tools to be moved weighed ≤ 10 kg and would require to be positioned on a track with a tolerance of only ±10 µm by whatever drive system was designed. On the *z*-axis, a carrier platform would be necessary to allow the polishing spindle to be fixed when the system was complete. The carrying capacity on the *z*-axis would need to be approx. 20 kg.
The commission thus included design, construction of a prototype, creation of a suitable control system, implementation of the interface to the tool drive, i.e. the polishing spindle, or possibly to a dosing system, and also the development of a graphic user interface.

Progress of Research

Within the project, the research is focussed on:

- working out the principles for the programming of the individual movements of the equipment, and selecting the relevant ones
- selecting the sensor principle, designing and constructing sensors plus related electronics
- 3D design
- construction of a prototype
- computer modelling of the equipment, design of controls for it and implementation of the real-time control system developed
- design and implementation of an MMI to be the interface between the human and the machine.

The drive as it is designed is well matched to the demanding specifications, on account of the impressive stiffness of the air bearings and granite base, and the choice of direct drive components for the drive mechanism. The air bearings and direct drives being a non-contact mechanism, they ensure durability, almost infinitely reproducible accuracy, freedom from stick and slip, and regularity in the movement trajectories.
When the drive concept and basic design had been arrived at and more or less completed, a start was made on working out the control system and designing the MMI in parallel to the building of the prototype.
The basic platform on which the control system was constructed was a conventional industrial PC in the 19’’ system with a DSP card (made by PMDi Ltd.) at its heart.
Much knowledge gained on the subject of which methodology to apply to the design of planar drives proved to be transferable to this project.
It is of advantage to use design tools like MATLAB or SIMULINK and their toolboxes to create models and simulate their functioning at

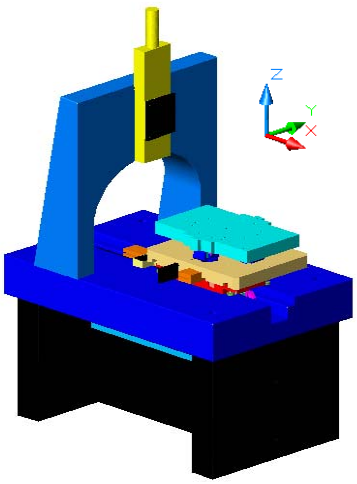

Fig. 1: 3D CAD view

a very early stage of the engineering.
By adapting the MATLAB toolbox known as RTW, or REALTIME WORKSHOP, to the hardware which is the target, i.e. the PMDi DSP board, the design process becomes consistent from start to finish, in that the program indicated will support everything from the graphic modelling through to the creation of the essential C code for the real-time DSP application.

The algorithm used to control the system (which must achieve track accuracy to within ±10 µm) follows a route probably hitherto unknown. The track control was on a closed loop basis and completely vectorial, relying on the fact that the kinematic values at any point on the trajectory can be analysed as having a deviation component and a homing component. If one calls this a “travelling co-ordinate pack” the calculation of the amount by which to regulate it can be carried out by a specialised structure for regulating the current state (effectively a virtual closed-loop cascade). What states are required will be determined by an observer.

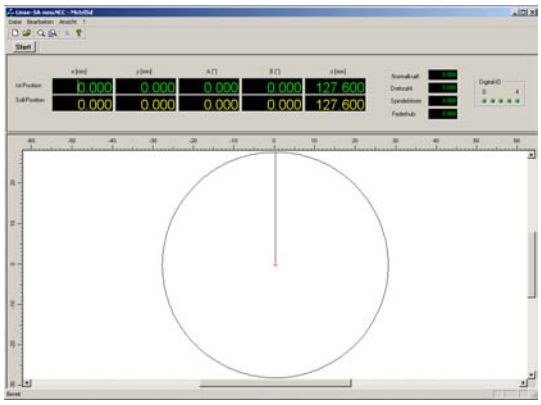

Fig. 2: MMI user interface

By clever use of limits within the closed-loop structure it is possible directly to affect the kinematic states, for instance ensuring that the ideal trajectory speed is maintained.
Experience had been gained on a variety of planar drive systems in the design and fine tuning of this special closed-loop algorithm. It must be said that new solutions had to be sought in the co-ordination of more than two axes, but these were, indeed, found in the course of the present project.
When the MMI user interface was being implemented, previously gathered experience from earlier projects again proved significant. The issues for representation and user-friendliness were largely dictated by the specifications set (and modifications requested) by the other partner in the project, who is at the same time the potential user and has the know-how and experience for the application.
Programs for the trajectory are described in G code (DIN 66025) and converted by a pre-processor into a format which the closed-loop algorithm will understand. The system includes the means of operating and monitoring the polishing process as well as displaying the ideal and actual positions and giving a graphic representation (see Fig. 2) of the projected ideal and actual trajectories for the particular plane.

Status of Research

The machine having been handed over to its user at the IMMS premises (see Fig. 3) and set up successfully in the clean rooms at Jenoptik AG before being commissioned, it is now having the drive system run through an additional test phase to confirm how the entire system performs when the tool drive is integrated. The test results are being evaluated by the commissioning partner. Details had not come through before we went to print.

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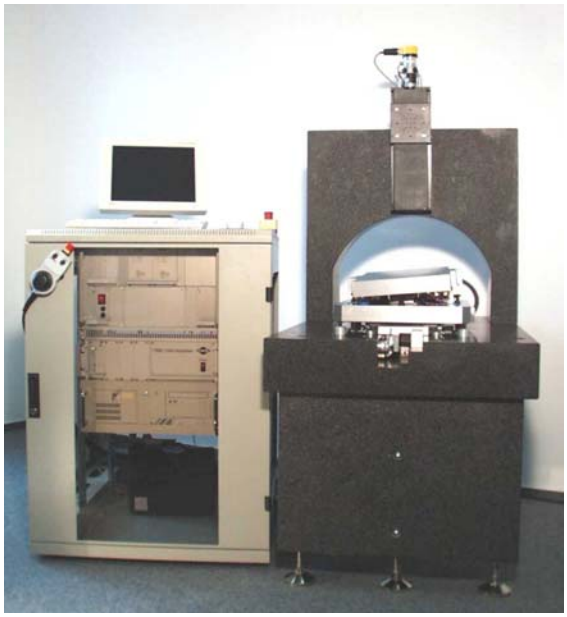

Fig. 3: The machine design put into practice

Designing a Measuring and Drive System for a High-Precision 3D Gauge

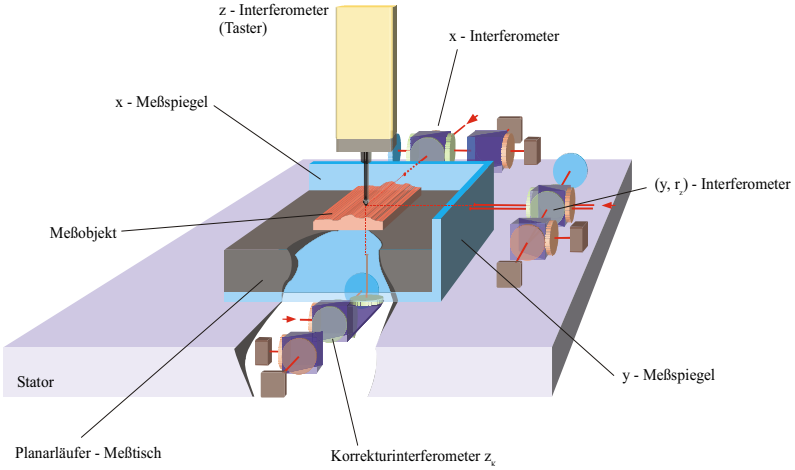

Fig. 1: Representation of the overall design for the precision gauge

Objective

It can be predicted for both general manufacture and the fields of micro-mechanics and microsystems that in future the registering of fine details of shape in ever greater complexity down to the nanometer range of resolution will be indispensable. There are, however, to date, no accurate high-resolution gauges available to carry out 3D measurement of bodies with linear dimensions between 0.1 mm and 1 dm. The current project is thus devoted to establishing the principles for such a high-precision 3D gauge. Certain designs for planar drives are being investigated which will accept simultaneous incorporation of laser measurement by interferometer into the overall design. Basic principles for the spatial measurement of bodies contained in a measured space of (100x100x10) mm^3 are thus being decided on. Supplementing the planar system with a probe based on laser interferometry for the *z* dimension of the samples produces the required 3D precision gauge. Drive solutions involving planar direct drives with air bearings are being investigated by IMMS in the context of a DFG (Deutsche Forschungsgemeinschaft) project. Two other partners in the project are the Prozessmess- and Sensortechnik FG (Research Group) and the Antriebstechnik FG, at the Technische Universität Ilmenau – whose subjects are, respectively, process and sensor measurement, and drive technology. One is tackling the layouts required for high-accuracy position sensing and the other the use of magnetism to move the objects through the measuring field.

Progress and status of research

The aim of the project at IMMS is to create a multi-axial direct drive with non-stick and non-slip glide, for a 3D precision gauge, to measure (100× 100× 10) mm^3. Such a concept requires the engineers to generate travel and movement (and the necessary forces) in a total of three linear axes (*x, y,* and *z*) and round one rotary axis (r_z). In the first (two-year) stage of the project, the *z* element is being registered exclusively by readings from a sensor mounted on a gantry. This sensor also registers if the stage itself changes in height on the *z* axis.
Figure 1 shows the CAD model of the gauge. It is a triangular lattice for the production of electro-dynamic force and moments in the *x, y,* r_z directions. The design selected has made excellent speed of movement possible at the same time as easy steering. It is characterised by optimum integration of all three drive axes into a system with a compact structure.
In the *x-y* plane, the forcer is guided on an air bearing, and it is turned round the r_z-axis by electricity. By this means, mechanical contact is avoided between the forcer and the stator. There is an option whereby the *x, y* guide elements may be replaced by a vacuum-preloaded version, which will reduce any nodding and rolling of the forcer during the acceleration stages. A schematic representation of the interferometric measuring axes is given in Figure 2. Their arrangement permits the object measured to be contacted (without there being any Abbé error) at the fixed point of contact while object is actually being moved.

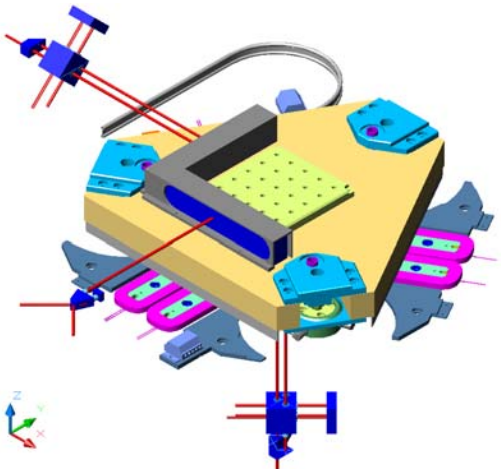

Fig. 2: Partial CAD representation of the measuring gauge with the 6D laser interferometer (shown without the stator)

Outlook

Work is currently being invested in a new design of cooling system for the actuators and in a system with which run-off errors on the part of the air bearing may be compensated for. These improvements will further increase the accuracy of both measuring and positioning.

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PMS100-3 precision positioning system

Objective

Today's machinery is often asked to position objects at high speed and with accuracy down to 1 µm, repeatedly following curved vectors with similar exactitude and high conformity on repetition. To meet these demands, there was a need to develop a system which was capable of later refinement to achieve ever higher accuracy.
The task was to produce the design for an device which included closed-loop control and the necessary programming, and to prove that it would function as intended.

Progress and status of research

Building on the symmetrical planar *x, y* positioning systems already developed at IMMS, it was decided to base the new design on a triangular forcer with a three-point airborne movement and the coils arranged in a star shape.

Fig. 1: Forcer viewed from below

Three photoelectric sensors are specially aligned to do the measuring in conjunction with a plane measuring grid to register the (*x, y*) position at a resolution of 10 nanometres.
3 linear motors act as the drive. Their actuator coils are fixed to a granite stator, and the permanent magnetic fields are provided in the forcer. Thus, the only connection which has to be made to the forcer is the 4 mm flexible tube bringing the compressed air. Cable harnesses are a hindrance to movement, and none is required in this design.
The base used for the drive is a granite block, approx. (600x600x120) mm³. The total weight of the drive is approx. 110 kg.
The system is suitable for use in clean-rooms.

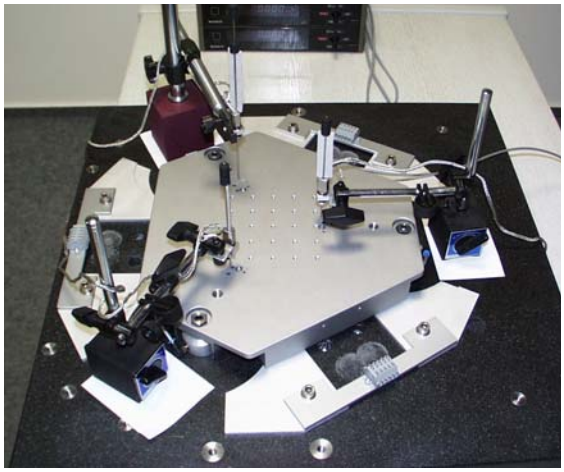

Fig. 2: Adjustment mechanisms for the measuring grid

Results

The field of action is a circular area 100 mm in diameter.
The drive will move objects of mass up to 5 kg with an acceleration of 2 ms^{-2}. Resolution of 0,1 µm is achieved for the position.
The high-performance DSP closed-loop control which ensures exact movement along the axes supports G code (DIN 66025) and HPGL. One system has already been created for Windows NT, and another is being developed which will run on RTLinux.

Fig. 3: Precision positioning system

Outlook

Work is being carried out on a yet more accurate version for the future which includes a calibrated scale resistant to changes in temperature. There will be a representation of the calibration functions in the open-loop section of the controls and the intention is to achieve accuracy of 0.2 µm across the entire range of travel.

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Design and modelling of drive systems for microtechnology (MODAN)

Objective

As part of the joint project funded by the BMBF (Federal German Education Ministry), IMMS is involved on two fronts. The first is the evaluation of simulation tools intended to support design engineering in the sphere of mechatronic drive systems. Specifications are to be derived from these investigations which will assist in further improvements to design methodology, with particular relevance to SimulationX (simulation software) and the SESAM programming system.
The second field in which IMMS is engaged for the project is that of the development of a variety of mechatronic drives:

- precision drives with a modular design, for instance electrodynamic direct drives and those based on magnetic resistance mini and
- micro drives, again modular, such as actuators relying on electromagnetic resonance or those on piezoelectric principles.

Investigations are also being carried out into this processing equipment under operating conditions when it is moving on five axes.
When the drive systems are being designed, the process follows the plan of deriving specifications for the simulation software from each step to assist in the next stage. Likewise, the outcomes from simulation are constantly compared with those which it is possible to obtain from developing and testing the drives under real operating conditions.

Progress and status of research

Working parties have been established from the very first so that the simulation tools can be evaluated in relation to particular drives. In parallel, the conditions were established for the designing and creation of the drives.
Many preliminary investigations were carried out with a range of experimental constructions and types of functioning, and from them has come, for example, the PMS100-3 planar electrodynamic direct drive shown in Figure 1. Currently, the Simulation X tool is being evaluated in relation to actuators relying on piezoelectric principles and the SESAM tool on those using electromagnetic resonance.

Outlook

The future will see a continuation within the project of this work on the drive systems. Further evaluation will be carried out in parallel and the data from the engineering design activities will be processed for use in the upgrading of the software.

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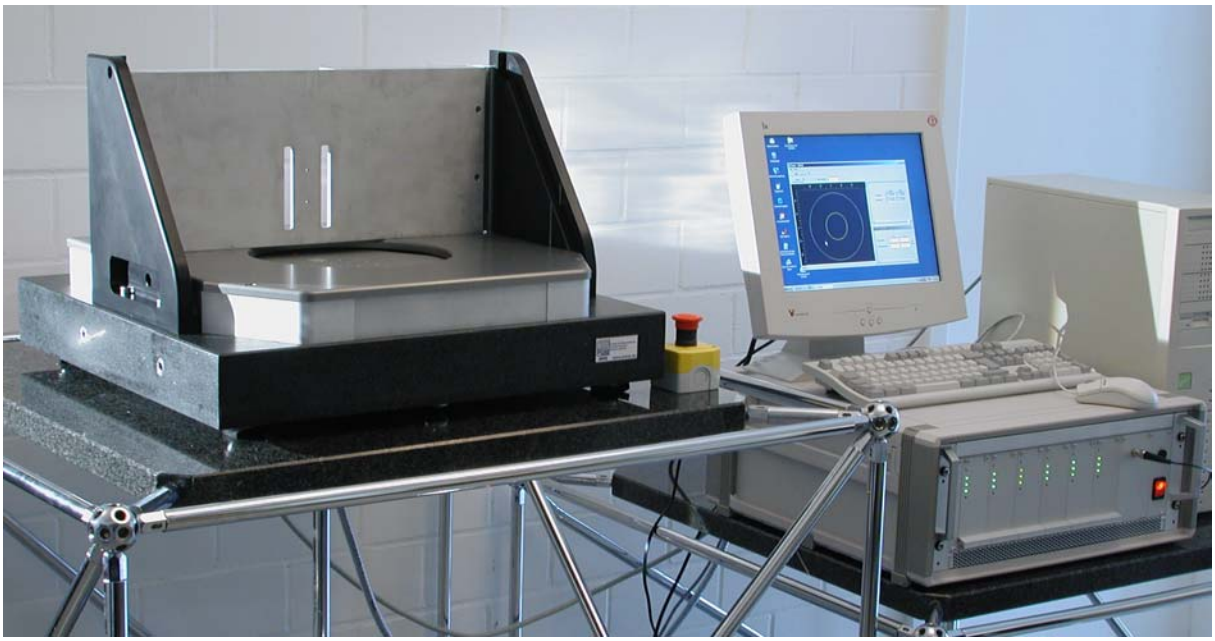

Fig. 1: Electrodynamic planar drive for use in analysis equipment

Development of a measuring gauge to investigate the flow properties of liquids

Objective

IMMS is participating in a European joint project together with two German companies, and a company plus a research centre in each case from Belgium, Spain and Switzerland. For IMMS the work involves developing and testing a gauge capable of measuring the micro-rheological features of films – a rheometer. The subject of the measurement is thin or viscous films of organic or inorganic composition. Not only is the measuring procedure being developed, but also a calibration method for the rheometer and fluids which can be used for calibration. The design for the device must include closed-loop control and the necessary programming, and it must be shown to function as intended. More is required: all the measuring equipment, data recording and evaluation programs must be capable of online connection and functioning so that their performance can be demonstrated in an online group testing session, a “ring test”.

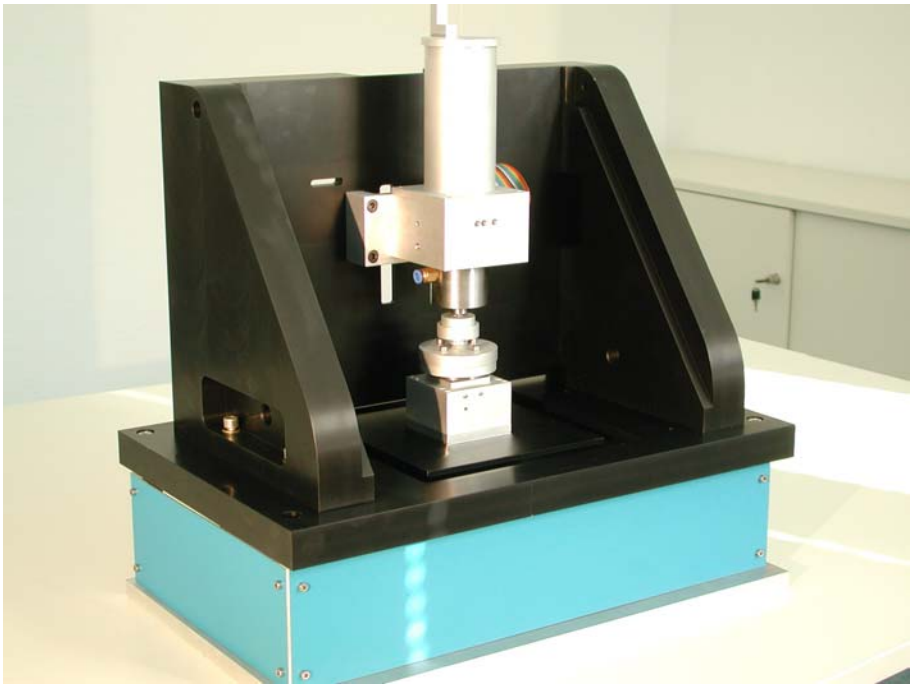

Fig. 1: Rheometer prototype

Progress and status of research

The starting point was the defining of the demands the rheometer must meet. The differing requirements of the project partners were taken into account: on the one hand, the conditions for a laboratory set-up, on the other, the fields of application and their needs. The detailed project definition was a reflection of up-to-date research outcomes in the R and D establishments and/or the specifications of the client partners, the manufacturing companies. Details had to be agreed of, for example, the lubricants (their viscosity, composition, etc.) to be investigated by the rheometer, what combinations of test subjects should be used (material, surface type etc.), and the experimental conditions (temperature, humidity, air pressure, mixture of ambient gas, length of test, etc.). The review of all these requirements led to a specifications list that was then the basis of the development of the device.

An initial prototype (see Fig. 1) had been created as a previous development task. The question of whether it would fulfil the specifications from the list was verified.

Outlook

Continuing work within the project will be the further modification of the device to meet the demands on it. One aspect is the method of recording, processing and graphically representing the measurement data, and a second aspect is the achievement of online working. The latter will require the gauge to be automatically controlled and the data to be conveyed over the Internet as measured, as evaluated or as graphically represented.

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High-precision planar step-motor drives with track control

Objective

Mechanical engineers all over the world are being required to achieve ever higher speeds and levels of accuracy. There is a trend towards the use of direct drives, which will avoid such problems of classic rotary spindle drives as free play and yielding characteristics. The fact that there is no gear box with direct drives reduces size and weight and improves the dynamics. In the attempt to exploit all the advantages of precision and speed offered by the design of direct drives, it is not enough simply to operate linear step motors in an open-loop control system. Closed-loop control of the drive is necessary.

As part of a joint project funded by the TMWFK, the Thuringian Ministry for Science, Research and the Arts, new-type, non-linear algorithms are being developed to regulate step motor drives. The need is to exploit the advantages of planar direct drives and at the same time achieve long distances of travel, relatively high speeds and great smoothness, whatever the velocity. To meet the need, models of the dynamics involved are necessary, together with ideas and algorithms for suitable and effective control systems. The main task being undertaken by IMMS is the development of multiple-axis feedback and control systems for track-setting. At present, the design of control systems which will permit the correction function calculated by project partners (specifically to assist in setting and following the track) to be implemented and tested is taking precedence.

Progress and status of research

The fundamental research is being carried out using a linear step motor as a first step. It starts up according to a computer-assisted DSP card made by dSPACE.

Control of the motor then proceeds with a cascade system that takes over the management of the position, the velocity and the acceleration. The implementation of the controller's concepts for the motor was first achieved using simple sine and cosine commutation for the individual phases; such commutation does not pre-suppose any knowledge of the actual force progression possessed by the motor and, for this reason, can quickly provide a control mechanism. In addition, a tracking of the commutation in proportion to the velocity was included in the control loop, enabling speeds of up to 700 mm s^{-1} to be reached. With this simple commutation, it was not possible at one and the same time to keep the position stable and the speed constant.

To achieve this high accuracy of position together with constant speed, knowledge of the real power of the motor is indispensable, and the only sure way of determining the commutation curves. To address the problem, IMMS' partner in the project, the Institute of micro system technology, mechatronics and mechanics (IMMM) of the local university (Technische Universität Ilmenau), has been carrying out simulation calculations for the interrelationship between force, current and position (F-i-s*), to enable a more accurate commutation curve to be produced. So that these outcomes from the calculation could be compared with real conditions, the F-i-s characteristic curves have also been determined experimentally for the individual phases of the motor.

On comparison of the measured and the calculated curves, close agreement of shape was found. It was interesting to note in respect of all measurements that the real forces were approximately 30% less than that calculated. Possible causes are changes in the working air gap due to the extended magnets, and/or the tolerances in the shape and/or deviations from the theoretical characteristic curves of the materials used.

Commutation curves were worked out on the basis of the data actually measured and then incorporated into the closed-loop control algorithm. In order that the quality of the commutations could be gauged for the type of motor being investigated, a procedure for comparison was developed. This is based on making a validation in respect of fluctuations of the controller's current under particular accompanying conditions, such as a good level of constancy for either velocity or acceleration. On this appraisment was based the choice of commutation curve for the motor. The control system features were brought even closer to the optimal by using an anticipatory control mechanism to reduce the ripple in the power (see Fig. 1).

It is necessary to take account of the fact that the commutation and anticipatory control are basically a reflection of static behaviour, while the closed-loop employed is at the same time affected by the system's dynamic features. This necessity caused the researchers to make a frequency response analysis for the control loop, the controlled system and the controller. The frequency and phase responses of the controlled system are depend on the motor's position; a periodicity of a eighth of the full step is characteristicly.Currently, the design of the control system is being adjusted to reflect this behaviour.

Outlook

As work proceeds, it will be necessary to develop an algorithm to identify the system and adapt the controls to the identification found. This process tends at present to be carried out manually, but could be largely automated, which would enhance performance.

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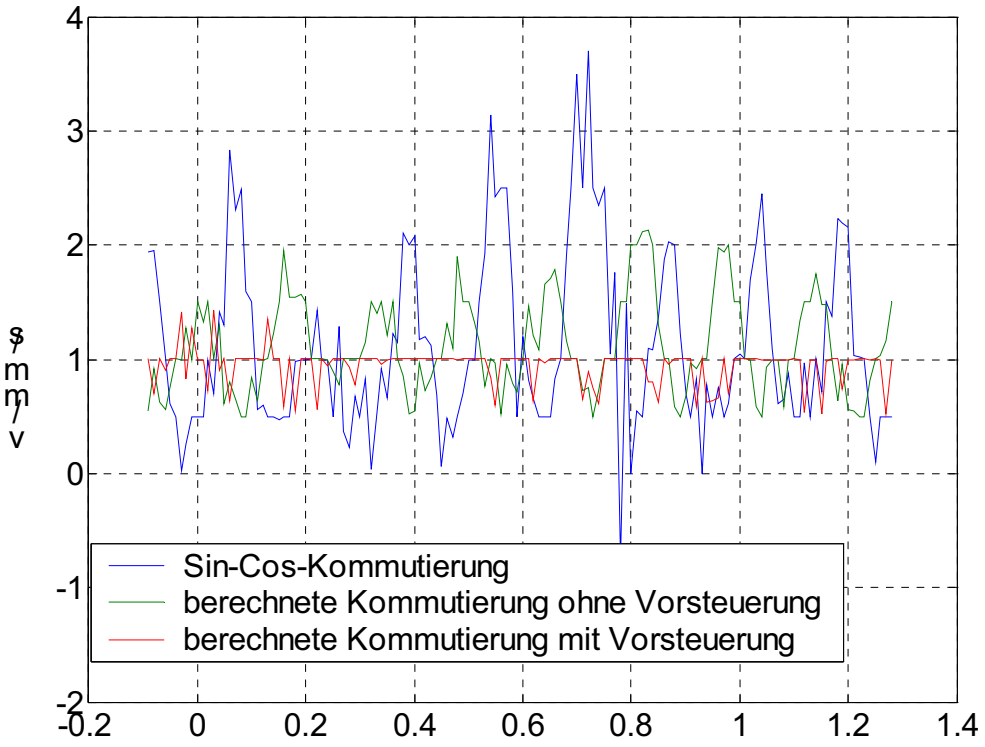

Fig. 1: Comparsion of the velocity constance while different stages of controller's development

System Design

The methodical and systematical design of complex embedded electronic systems serving many different industrial and research fields is still, as it long has been, one of the greatest challenges confronting the electrical and electronic engineering branch of industry as it develops. The task is constantly increasing in complexity. Traditional engineering ideas are being modified and even replaced by design processes at a new qualitative level. In using them, the priority is to model the complex system to be designed as early as possible. From the model follows verification, ideally using abstract and formal design methodology. The System Design Department is addressing these issues by using such up-to-date tools and methods for modelling as Matlab/Simulink or Unified Modeling Language (UML).

Within the **Digital Signal Processing and Industrial Electronics** section**,** the use of innovative modelling methods in SystemC™, above all, has raised the work on problems of real-time image processing with co-designed hardware and software to the new level of quality. It has proved possible to develop a method of combining optimised hardware operators into the system level without specialised knowledge of implementation being required. The benefit is that new applications can be developed for the field of industrial image processing with far less effort than previously. In the Sensor Science part of the section, solutions have been developed which make signal processing (i.e. calibration, linearisation and compensation) for capacitive sensors possible in the close vicinity of the sensor, together with the coupling of the resulting data to a standardised digital bus interface (IEEE 1451, SPI). Verilog und VHDL were used for the implementation.

In the **Buses and Networked Systems** section, the concentration has been on cutting-edge real-time communication technologies to support industrial communication and automatic machinery. This enabled the bus converter project, begun in 2001, to be extended with new technologies such as IEEE 1394b and USB 2.0. The section gave a lot of its attention to the subject of real-time-capable* communication in industrial settings (see page 17). New routes were taken to find state-of-the-art, real-time solutions with a broad band and genuine practical usefulness to add on to such conventional technologies as field buses or even take over from them. Particular examples are the 1394b technology already mentioned, and solutions devised for real-time Ethernet use. Embedded Linux is increasingly used to implement such communications solutions. This gives all the benefits of an innovative, open-source operating system with no licensing charges.

The section further concentrated on improving the S-ATA IP core (see page 17). S-ATA is a new connection norm for IDE hard drives. It is excellent as a hot-plug and has outstanding resistance to interference. By implementing the IP core in VHDL, the preconditions were created to enable this technology to begin to be applied in embedded systems.

In the **Embedded Software and Automotive Systems** section, problems arising in model-based design of complex embedded systems are the chief subject of investigation. The potential applications extend from the electronics in motor vehicles to industrial process control systems and telecommunications. R and D work shared with an industrial partner making smart wireless communication devices continued during 2002 with considerable success. It involved extending the software and hardware platform (which includes hardware-independent middleware for use in intelligent GSM/GPS modules) on the one hand, and, on the other, investigating methods and tools for model-based design (using UML) in this field of application. The approach to modelling which was used was based on the idea of a product line, leading to the design of product families. It was thus closely related to current developments in software engineering. The longstanding co-operation with automotive manufacturers on electronics for vehicles was also maintained. The focus has, for some considerable time, been on integrating model-based design tools into industrial design processes and optimising the interfaces within the processes. In addition, an experimental vehicle has been developed for research and demonstration purposes. It is fitted with a great many actuators, sensors and control mechanisms which are networked by means of bus systems. The vehicle was first presented at the SPS/IPC/DRIVES 2002 as a demonstration platform for the solution IMMS had developed for an intelligent CAN Ethernet gateway (see p. 17).

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Demonstration of methodology and technology for networked embedded systems

Objective

Embedded systems are increasing all the time quite dramatically in complexity. The trend is being forced by customer and user demand. The resulting constant increase in the range of functions to be provided by these systems requires, in particular, new sensor and semiconductor technology, ever more networking between subsystems, and a growth in the use of software-based solutions.
Management of this complexity is putting new demands on design engineering and tools, for those used to date are increasingly proving inadequate. The deficit is expressed in several ways, among them rising development costs and increased reliability problems. The need for action is most felt in those industries using the applications where both cost and safety are at issue, such as the automotive field.
An approach which promises well for the reduction of the problems mentioned is model-based design of embedded systems. The modelling procedures and tools, and those for the abstraction, verification, and transformations of systems, all require rigorous emphasis on the early design stages – those of modelling and verification. At the same time they offer the possibility of automating the later design stages – those of encoding and testing.
As the origins of model-based design processes lie in the fields of business software or electronic design automation, there is currently a huge demand for methods adapted for the engineering field, and likewise a need for experience in the use of these methods to create embedded systems. A demonstration model produced by IMMS to exemplify methodology and technology deals with these issues. It is a suitable research platform because it has the typical features of this class of systems: functionality, sensors and actuators, interfaces, bus systems, hardware and software platforms and the complexity that all these features imply.

Progress and status of research

As IMMS was already active in the automotive field and had some preliminary work, the choice fell on a demonstration vehicle and, more precisely, upon a radio-controlled model truck, as this afforded a good compromise between all the factors of cost, size, space required, presentability and functionality. The vehicle is electric-powered, with a cab front and an articulated container base behind, on a scale of 1:15 (see Fig. 1). The various actuators, sensors, electronic control systems and electrical supply connections are distributed over both cab and trailer. The semi-trailer section affords enough space for the various sub-systems, with some to spare for later extensions. As the vehicle will actually move when “driven”, its features encourage meaningful use of such functions as a anti-slip regulation(ASR). The vehicle is also equipped with full lighting, among other things, including a system for recognising if any lights are defective, and a theft alarm. It is possible to add modules to assist with external communication (WLAN, GSM), a bus gateway (CAN, Ethernet), a navigation unit which uses GPS, and further sensor units to register such things as acceleration, temperature, angle of rotation and lights.
The vehicle has “by-wire” systems which replace the conventional, exclusively mechanical or hydraulic, mechanisms of the steering, brakes, gear box and so on. The electro-mechanical solution is either added on or totally replaces the old one. Measurements and values required for control are transmitted between the components of the system via buses.
The control devices, which are effectively computer nodes, are connected to the actuators (e.g. drive control, steering servo assistance, lights) and to various sensors (for e.g. wheel revolutions or switching contacts), and they exchange necessary information using a CAN bus system (see Fig. 2). The

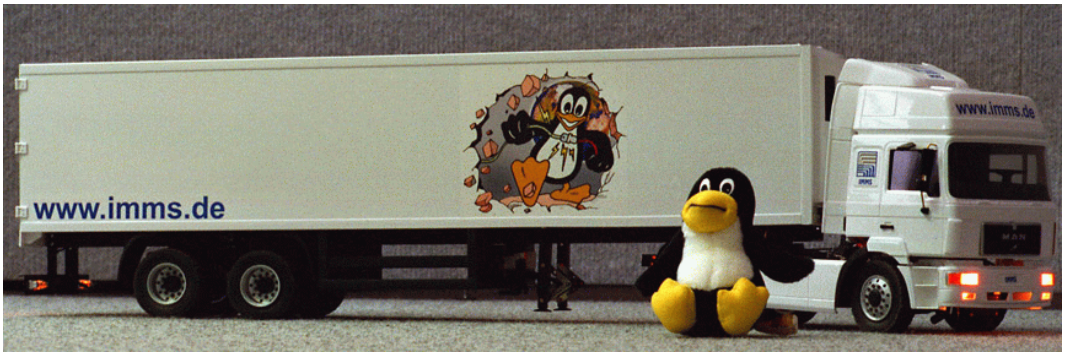

Fig. 1: demonstration vehicle

functions (e.g. anti-slip regulation) are then realized by the software within the control devices. These are equipped with a real-time operating system, OSEK, with relevance for automobiles. As part of a current IMMS research project, the demonstration truck has been extended by an intelligent bus gateway for CAN and Ethernet applications (see Fig. 2). This gateway has its own embedded web server, based on Linux, which permits direct access to the vehicle's internal bus. The truck is connected via Ethernet (and a wireless LAN) to the external world. This permits a standard desktop PC to access the vehicle data using a web browser. The solution was successfully demonstrated at the SPS/IPC/DRIVES 2002 trade fair.

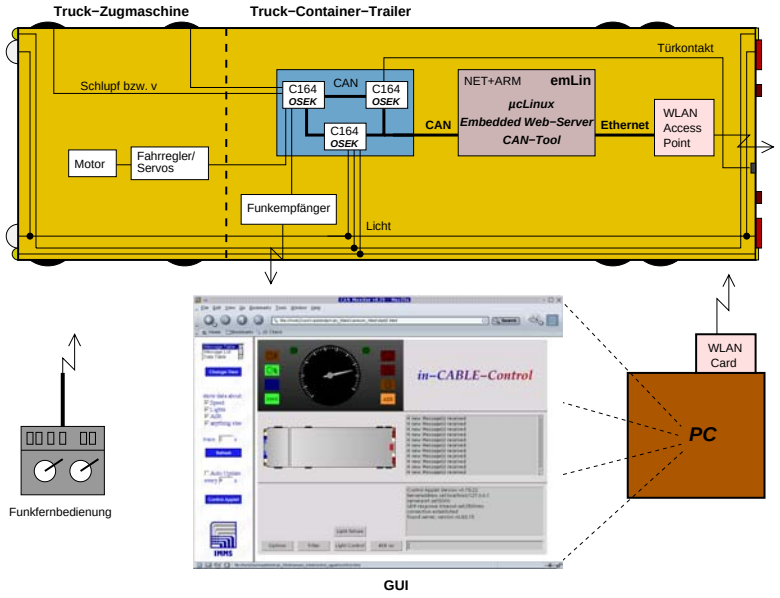

Fig. 2: Components and construction of the demonstration vehicle

Outlook

Continuous work is being done on the demonstration model as presented here. Functions and sensors will be extended in the future. Additionally, it is being made possible for the actuators and sensors inside the vehicle to be accessed through the above-mentioned intelligent bus gateway directly from design tools which have been based on the model. The design engineer thus has the chance of validating his or her model at a very early stage using real hardware components.
In work on the methodology, the focus is largely on UML for embedded systems, formal verification techniques, and the design of distributed control systems. Investigations being carried out in parallel are concerned with innovative design tools and their practicality in relation to embedded systems. Our aim is to use them in a way suitable for industrial engineering processes.

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Implementing Serial-ATA in the FPGA for embedded systems

Objective

As large quantities of data have to be stored in ever shorter times, ever faster mass memory interfaces are coming to be required. The hard-drive interfaces currently in use (UltraATA100 or ATAPI 6) are at the practical limit of their data storage rate because of their parallel architecture. The summer of 2001 therefore saw the launch of a new norm, the Serial-ATA, with which the data are transmitted in series.
The intention is that this new bus should be used exclusively as an internal one. By using LVDS technology the data transfer on a Serial-ATA cable is particularly resistant to interference. Instead of 80 wires (UltraATA100), only 6 are necessary. In the first version the max. data-rate is 150 megabit per second net (1.5 gigabit per second gross). In addition, the new standard should be absolutely compatible from the software point of view with the standard used to date, so that the same drivers can be used.

Fig. 1: Logo for the Serial-ATA standard

The reduced power consumption and the hot-plugging facility (the method of storage can be changed even while the operating system is running) make the Serial-ATA interface eminently suitable for embedded systems.
A research project commissioned by TMWFK, the Thüringen Ministry for Science, Research and the Arts has developed an intelligent bus coupling system. There was a wish to extend this by a mass memory interface (see Fig. 3), in which the new standard would be used. The Serial-ATA host function is assumed by an FPGA on the board. This requires the development of a universally applicable Serial- ATA core using VHDL programming language.

Progress and status of research

The protocol for the Serial-ATA standard is made up of several layers: physical, link, transport and application. It is necessary to clarify in advance which parts of the protocol are to be written in VHDL and which are available already as hardware, or even software (in the controller).
It has been shown that the physical layer cannot be realised in an FPGA and so must be provided as external hardware for the purpose. However, there are still no physical layer chips for Serial-ATA available. To be able to test the transmission route despite this, a physical layer has been constructed using a serialiser chip and a PLL chip. Unfortunately, it has become apparent that this variant is not suitable for a Serial-ATA physical layer. The gigabit Ethernet transceiver chip offers a better solution. This physical layer chip already contains the channel coding (8B/10B) and has a 16-bit data interface with the link layer. It also has the maximum data rate as required, 1.5 gigabit per second, though the command codes it uses are slightly different from those of the Serial-ATA "phys". So that this chip could be used despite the differences, the command code generation was modularised and adjusted accordingly.
The link layer has an acknowledgement system for the receipt of commands and data. In the same way, a CRC32 check on the total for the incoming data is calculated and then compared with the total sent at the end of the data stream for this checking purpose. To block the check figure and command codes off from the actual data, some sort of "pipeline" with control-state-machine is necessary. The requirements for flipflops are thus increased (see Fig. 2). The FPGA to be used must have enough area to meet these demands.

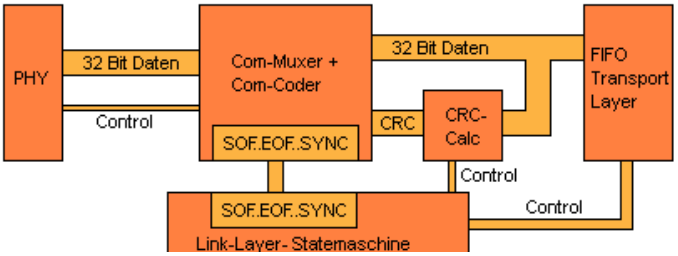

Fig. 2: Circuit diagram for the link layer

The register data of the application layer are "packaged" into frames in the transport layer and sent to the link layer as frame packets – and vice versa. Again, some sort of control-state-machine is necessary to make this function possible. The Serial-ATA standard defines eight different types of frame, each of them clearly recognisable from the 0 byte. When the frame recognition is implemented, IF-THEN

trees are created, which can lead to timing problems at the synthesis stage. It may be necessary to unravel the VHDL code and separate it into sub-modules.
The link layer and the transport layer were implemented as VHDL cores in FPGAs. The application layer is better realised in software on a controller, as it is physically close to the driver. The compatibility of Serial-ATA with the "old" software driver is achieved by using an identical register set to that used by the previous UltraATA 100 standard.

Outlook

In 2003, by means of a converter board, a "classical" hard drive will be capable of use as a mass memory. A flash memory is also to be created with a Serial-ATA interface.
So that the Serial-ATA interface can also be used in conjunction with future ready-made products available on the market, such as Serial-ATA drives, the original physical layer chip will have to be connected to the FPGA and the link layer adapted accordingly.

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Fig. 3: Demonstrator with simulated Serial-ATA-drive

Real-time image processing using hardware and software co-design

Objective

It is the trend for automation, quality control and quality inspection in industry to require the use of sensors which function in real time. It is also necessary for the sensors to cope with ever greater quantities of data. Solutions that only make use of software are often inadequate to the task even with the most powerful of processors – an instance is 100% inspection of goods being produced at a fast rate.

If the option is taken of parking function blocks in hardware as part of a co-design and running hard- and software in parallel, sensor signal processing can be made much more efficient.

A research project commissioned by TMWFK, the Thuringia Ministry for Science, Research and the Arts, is providing the context for the development of machine vision systems which rely on a platform with a hardware and software co-design. The plan includes not only the construction of prototype hardware, but also, importantly, design methodology. The engineer for an application will often have specialist knowledge (of, for instance, image processing), but rarely have knowledge of how to design hardware.

The method developed has made it possible to include hardware functions at the abstract level without any specialist knowledge of implementation. The effort required for the development of new applications is thus reduced.

Progress and status of research

The project began with the design of a demonstration platform for image processing applications.

The platform is shown in Fig. 1; it has the addition of a PCI plug-in card made up of a standard DSP and programmable (FPGA) hardware. Within the FPGA a circuit has also been created to manage flexible data streams and exchangeable mathematical operators for image processing. These operators are coupled direct to the input data stream. To allow the operators which work with local environments to function, an external memory (line FIFO) is provided (see Fig. 2). The signal processing takes place while the image is being registered and transferred by the camera to the external graphics memory. An image processed previously by the DSP or the PCI bus can be read in parallel. Not only the straight image data, but also events arising at other times – such as the co-ordinates of the pixels for the object – can be stored in an internal FIFO.

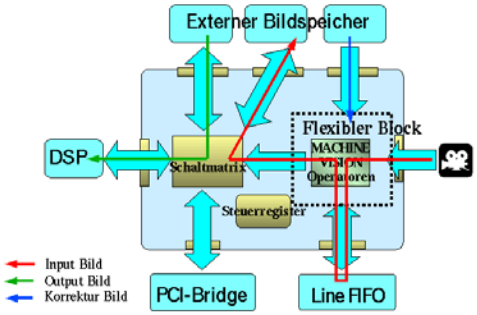

Fig. 2: Topology of the FPGA

The project has, further, involved establishing design methodology for the hardware platform. The industrial partner in the research is TechnoTeam Bildverarbeitung GmbH, and they already had a tool for designing and simulating software-based image processing systems. This tool enables a variety of function blocks and algorithms (stored in libraries as C++ code) to be united on one interface as a data flow graph. The model is executable and can be checked out by means of simulation.

The toolbox has been extended in the present

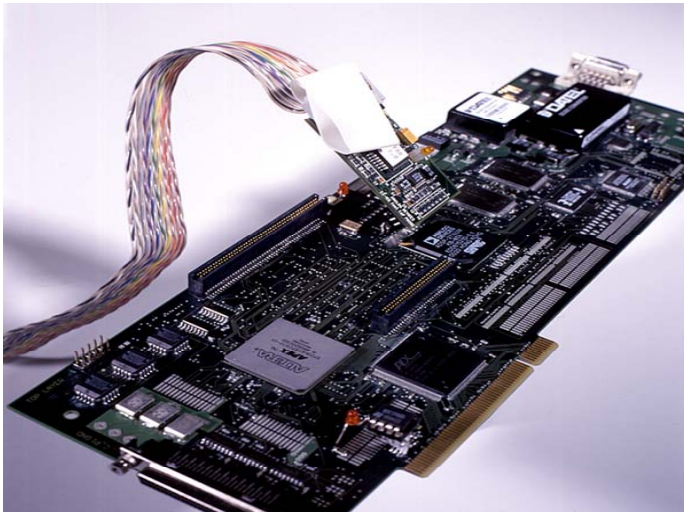

Fig. 1: PCI demonstrator board

Components of the prototype:

- General Purpose DSP (ADSP 21160 with JTAG debug interface)
- Hardware-based co-processor (implemented in an APEX20KE400 CPLD)
- Memory (3 x 2-Mb graphic memories,
- 64k x 64-bit line FIFO)
- Camera interface (2x12-bit cameras)
- DSP interface (addresses 32 bit, data 32 bit) Communications interfaces (IEEE 1394, RS232 interface)

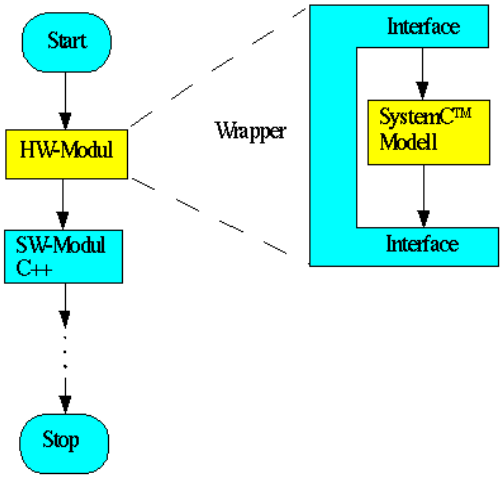

Fig. 3: How hardware modules are combined into the system model

project to enable systems which include both hardware and software to be realised with it. The libraries already to hand have been supplemented with mathematical hardware operators which can be simulated and loaded into the FPGA. Using SystemC™ has made simulation of the hardware modules executable with exact replication of timing and bits. A C++ wrapper has been used to integrate the SystemC™ operators into the system model (see Fig. 3). There is a VHDL implementation reflecting its behaviour for every operator.

The method makes it possible to use both hardware and software components very easily within a single system model – i.e., to put co-design into practice. The image processing engineer has recourse not only to a tried and tested library of operators but also to new operators which can be included for the particular application. This is done by taking a basic operator which has been provided as a template and making it into an operator with a new function. The relevant C++ code can then be used by a hardware specialist as an executable specification for the hardware design of the mathematical operator. He or she then provides the system engineer with a refined model for use in the verification of the final whole system.

The design flow for the codesign is as follows:

1. Create abstract model of system
2. Verify by executing (simulating) the model
3. Partition the model by inserting hardware operators already available, create new hardware components using the C++ template
4. Verify again (by simulation) – this time with the refined, partitioned model
5. Download the model into the DSP and FPGA
6. Verify the “real” system.

Outlook

The design methodology here presented is tailored to fit machine vision applications. It is the aim of the project to extend the procedure to be of relevance to other fields of application Matlab/Simulink is often used for designing signal processing systems, those which are in close proximity to the sensor, for instance.

So that the many functions made available by the numerous Matlab libraries can be combined with the advantages of hardware modelling that has timing and bit accuracy, a framework has been created which permits SystemC™ functions to be linked into Simulink models (see Fig. 4). The hardware models are included as Simulink S functions and the transfer from the Simulink simulations to those of SystemC™ takes place by means of a wrapper. This manner of proceeding ensures that all the operators from the project above are re-usable. Development of new hardware operators for image processing with Simulink thus becomes possible.

By coupling the two tools together as described it is possible to check out a later hardware implementation on the basis of a Simulink model. A planned step for the future is establishment of code generation for the hardware modules. By combining the tools developed so far with Mathworks’ Real Time Workshop, it should be possible to carry out a start-to-finish model-based co-design from Simulink as starting point.

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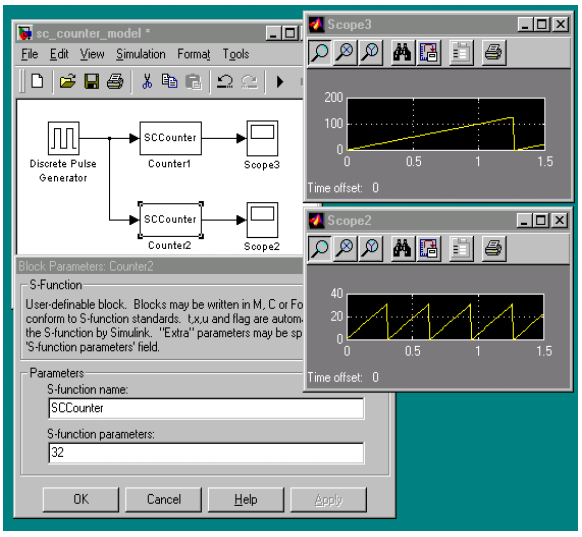

Fig. 4: System C™ as a Simulink S-Function

Microelectronic Circuit Engineering

This Department has concentrated in 2002 firstly on developing and application of new design methods so that on-chip systems (SoC) can be faultlessly produced – methods include VHDL-AMS and symbolic analysis; also embedded DSP systems. The second focus has been optimising integrated analogue circuits, which has involved transimpedance amplifiers, ADCs, optoelectronic sensors and SOI circuits.
IMMS is working on innovative applications in:

- SOI circuits for high voltage and high temperature applications
- SC sensor amplifiers
- ADC design
- optical communication, optical sensors, DVD reader units
- synthesis of mixed-signal ASICs and embedded systems (based on DSP and controllers)
- formal verification and simulation of mixed signal circuit design
- symbolic analysis of analogue circuits.

The research results achieved have led to intensive joint efforts with semiconductor industry, design centres and users of sensors and electronics. The various funding agencies for the research are the EU (the MEDEA+ programme and FP6), BMBF, the German research council EDA-Centrum (Ekompass), the BMWi, the German research cooperation AiF (VDMA/DFAM), the TMWFK – Thuringian Ministry for Science, Research and the Arts, and the TMWAI – Thuringian Ministry for Industry and Employment and Infrastructure.
Following are mentioned some of research results for 2002:
In continuation of works on RF circuits we have developed integrated inductances and circuit blocks for 1-GHz transceivers as a main focus. Industrial works are made on SiGe technologies.
The ADC section addressed the new subject of capacitive sensor electronics (see p. 24). This project is producing solutions to the problems of sensor electronics for a wide range of sensors including those for moisture and pressure. Sensor amplifiers are being developed, and work is being done on AD conversion and signal processing.
The optoelectronics section has made research on DVD reading units for blue light (see p. 28). The DVD reading circuit speed and their sensitivity were further increased (TIA* with bandwidth > 100 MHz). For read-write operation, circuits with variable sensitivity have been developed.
The “circuits for optical low-cost buses” project is presently exploring optical connections with immunity to interference. The project makes designs for the appropriate transmit and receive amplification for multi-mode fibres (see p. 30). The original goal for transfer rates around 155 Mb/s has been expanded in the current work to a range between 625 Mb/s and 1 Gb/s at light wavelengths between 600 nm and 850 nm. Design methodology to enable a system to be described and simulated in mathematical terms (MATLAB, SIMULINK) has been researched for embedded mixed signal systems, and from the simulation and optimised solution for the electronics has been derived (see p. 34). The method permits subsequent implementation either with controllers, with DSPs, in an FPGA or as an ASIC. A workshop in November 2002 presented a summary of the results, to allow those interested to make swift use of them.
The research on SOI circuits positively stormed ahead (see p. 38). The models and sub-circuits which had been tested out in 2001 when an analogue and mixed signal SOI design kit was produced for X-FAB Semiconductor Foundries AG, Erfurt, formed the basis of intensive research on control circuits and power drivers for the automotive field. The raising of the temperature for their application (to 220 °C), their latch-up immunity and their resistance to ESD all render them of much higher quality and reliability than the technologies previously available. Work is continuing on SOI RAMs and SOI Hall elements.
In a number of projects, EDA design methods were the continuing focus:

- ASDESE: ESD modelling
- ANASTASIA: mixed signal design with behaviour description languages, symbolic analysis, technology transfer (p. 26)
- VALSE: formal verification of mixed signal circuits (p. 34)
- SPEAC: simulation of heterogeneous systems (p. 32)
- DFAM/DSP: systematic mixed signal system design

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New design methods and new designs of high accuracy SC A/D converters

Objective

In 2001, the ADC (analog-digital converters) group concluded successfully its project called in German "Entwicklung von A/D-Wandlern für die Anwendung in Digitalen Signal-Verarbeitungssystemen unter Berücksichtigung neuester Technologien, Techniken und Anforderungen", which was supported by the Thuringia Ministry of Science, Research and the Arts under the grant number B609-97049 and concerns the development of state-of-the-art analog-digital converters. The resulting prototype was a cyclic RSD ADC which was realised in CX06 technology (manufactured by X-FAB AG Semiconductor Foundries, Erfurt) and fully evaluated. In the following year, 2002, a follow-on project has enabled the characteristics of the ADC to be further improved in respect of linearity, sampling rate and noise purity, so as to benefit for complex sensor applications.

Progress and status of research

Within the project, design methodology to use for swiched-capacitor (SC) systems has been systematically established and made effective and reliable. The potential of the VHDL-AMS hardware description language has been explored in respect of the modelling of mixed analogue and digital systems using the AdvanceMS tool. There is a particularly tough challenge to be met in designing switched-capacitor systems for high accuracy ADCs, and this is that correction mechanisms have to be applied to compensate for the errors caused by the operation amplifiers which are required – especially finite gain and DC-offset. Placing correction mechanisms within the analogue processing part of the switched-capacitor circuit system avoids the huge digital correction calculations which would otherwise be necessary to enable the linearity demands for resolutions above 11 bits to be met.
At the conference ADDA'02 , which was held on June 27th and 28th, 2002, in Prague, a correction method already tested out in practice was presented.
Use of this correction led to clearly improved ADC linearity. However, contrary to expectations from simulation, it has not yet been possible to attain linearity appropriate to 14-bit resolution. The main problem is that complete simulation of the characteristic curve of the data transmission cannot be achieved in an analogue simulation at the transistor level (net-list). ***Modelling behaviour with VHDL-AMS***

To find any errors in the A/D converter's switched-capacitor system design, much faster simulation methodology is required so that the charge transfer behaviour and any errors caused by the non-ideal OpAmp (and the correction mechanisms for these) can be properly modelled. To this end, the general solution was laid out mathematically for the steady-state of the charge transfer behaviour in switchedcapacitor circuits, with any number of capacitors involved, and assuming the OpAmp suffers from offset and has finite gain. Then a modelling algorithm was established for VHDL-AMS in the sampled-data Z-domain, using REAL SIGNALS.

A generator for a SC behaviour model in VHDL-AMS

To convert complex switched-capacitor systems developed manually into the necessary VHDL code would open up possibilities of error which would be unrecognisable to the VHDL interpreter. An automatic conversion routine was created, a) to permit simple notation of the basic sampling and charge transfer operations within a clocked system and b) to convert them into VHDL with the aid of an AWK scripts.
Using this tool also provides two further advantages to the design flow, each relevant to effectivity and reliability:

- Within a short time, a variety of conceptual switched-capacitor solutions to a problem can be described, verified and compared with each other. If the method used involved schematic entry (CADENCE) – including switches, capacitors, OpAmps and all the associated control logic for the clock phases – followed by the relevant simulation, not only would vastly more time be needed, but also errors would be likely and it would be impossible to do comparative modelling of varying designs.
- The conversion procedure using the VHDL-AMS generator enables a number of plausibility tests to be integrated in the form of alarms and error messages which can be triggered at the level of the abstract switched-capacitor system level, signalling any errors or risky circuits there. An example would be an alarm built in for the use of two integration capacitors for one OpAmp in the same clock phase.

Outcome of the SC-behavioural simulation

The simulation of the whole ADC characteristic curve only took 10 minutes (at a 16 bit resolution!) and virtually the same degree of error was found as on evaluation of the actual measured values from prototypes. The varying of the error measuring capacity to correct the OpAmp error resulted in an optimal value of $2.5 \cdot C_x$ (C_x = value of the operating capacitors),

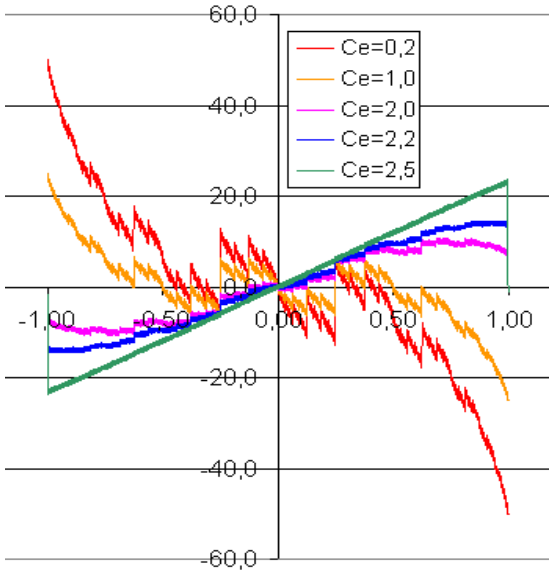

Fig. 1: Complete simulation of characteristic curve for the INL of the ADC (shown: LSB error at resolution of 15 bits) with various correction capacitors (the one realised was 2.2 pF)

in contrast to the value previously assumed, which was 2.0-times.The work also included simulating an overall gain-slope error for the characteristic curve, and this was also vindicated by the measurement actually taken. This error has the effect of causing a difference in scale as against the reference voltage.

This new design methodology brings with it two new switched-capacitor systems which prevent both of these inadequacies occurring and, furthermore, can be completed only within three clock phases per bit cycle. Both these systems have been successfully verified at the SC-system level using the new design flow.

A generator for a SC structure model in VHDL-AMS

It is, of course, still possible for the mathematical behavioural modelling to contain errors. Comparative netlist simulation of the SC-transients obviously is necessary. To meet this need, a VHDL-AMS generator was created to produce a structural model consisting of switches, capacitors, and OpAmps. The starting point was the same notation as used for the SC phase operations. By “mixing” both of the models generated, a procedure which can be done quite elegantly with the assistance of VHDL-AMS, the necessary comparative simulation could then take place.

New SC system concept for cyclic RSD-ADC

In the new SC system design, the Sample-and-Hold block is replaced by a second arithmetical block, which likewise produces one bit. This results in a two-stage cyclic pipeline architecture. Correction of the OpAmp’s error takes place using a mismatch-independent voltage addition correction procedure. The principle is also mismatch-independent in regard to all incoming (V_{ref} and V_{in}) and circulating signals.

Each conversion cycle requires six clock phases per bit. The pipelining by two phase cycles overlapping, only three clock phases per bit resulted for the output. With this principle, a fully differential SC design requires 20 capacitors and 120 switches.

The second SC design has the classic structure with both. the Sample-and-Hold and the arithmetical block. Correction of the OpAmp’s error takes place using the charge addition procedure. It has been possible to compress the correction clock phases to such an extent that, again, only three phases per bit are required. The disadvantages mentioned above can be avoided by, for example, proving what size the necessary error measurement capacities should be, using behavioural simulation with VHDL-AMS. One outcome is C_e=2.03*C_x, an ideal correction ratio.

With this principle, a fully differential SC design requires 18 capacitors and 92 switches (compared with the ADC2 prototype, which required 20 capacitors and 96 switches). The advantage over the two-stage cyclic pipeline architecture is that fewer components are required. Some disadvantage comes from the additional matching necessary in respect of the error measurement capacities. If the relative matching error does not exceed 1%, linearity is

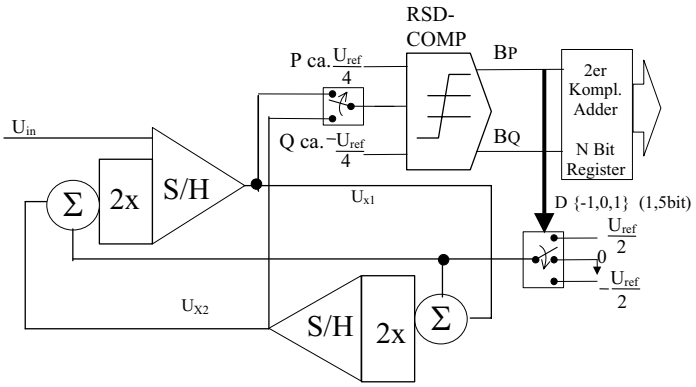

Fig. 2: Circuit diagram for the principle of the cyclic two-stage pipeline RSD ADC

achieved for 14-bit resolution.

Outlook

It is intended to decide between the two and use one of the two switched-capacitor ADC systems in 2003 for the chip prototyping within the project named above.

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Symbolic analysis of analogue circuits

Objective

When analogue and digital systems are being designed, the simulation of electrical networks is at present mainly carried out using numerical programs such as SPICE and Spectre. These programs are capable of simulating the circuit behaviour with great accuracy before manufacture commences, saving time and money.
The results of the simulation are in the form of tables or figures and can be represented in diagram form. However the results hardly permit any conclusions to be drawn about the relationship between circuit features and design parameters. Repeated simulations will still only indicate the influence of the individual parameters in a limited fashion. Thus, numerical simulation here becomes more or less a verification tool. Yet the early stages of design engineering require attention to qualitative relationships, which can only be obtained by analytical calculation.
This form of calculation is still not very common on computers and has tended to be performed manually up to now. In practice, its application is thus restricted to simple circuits, as the complexity of the transfer functions increases very rapidly with the number of components.
A new approach has become possible since ITWM developed the “Analog Insydes” for symbolic analysis. This has been made available to IMMS within the *ANASTASIA* research project. Analog Insydes is implemented as an add-on to Mathematica, the computer algebra program.

Symbolic Analysis

Symbolic Analysis starts out from a netlist with symbolic element parameters. The list can be created with a text editor or imported from SpectreS (Cadence) or SPICE netlists using an additional module. It is useful first to run the simulation numerically to ensure that the end result agrees with that of the numerical simulator (see Fig.1).
Exact symbolic analysis is neither possible nor reasonable for anything but small circuits, as the complexity of the transfer functions rises exponentially in relation to the number of elements on the netlist. Analog Insydes offers a range of approximation procedures which simplify the transfer functions (by ignoring insignificant coefficients) to such an extent that qualitative evaluation is possible.

Progress and status of research

The first use of Analog Insydes at IMMS was to analyse a TIA (transimpedance amplifier) in the amplification circuit in a DVD reader. The main goals of the optimisation were to increase the bandwidth and to remove a resonance peak. The Infineon module was used to import the netlist in the SpectreS format. Some manual adjustments were necessary. To reduce the complexity of the equations, a number of parts of the circuit were replaced by simpler models. Using matrix approximation, it was possible to calculate definitive transfer functions.
Relevant parameters calculated were the capacity of a coupling capacitor, and the gate capacity of a level shifted transistors.
When the coupling capacity has been eliminated and the transistor size reduced (see Fig.2), simulation reveals that the bandwidth has been increased by 23 MHz, the resonance peak reduced, the group delay improved, and the transient response also improved.
Further analyses were carried out with a folded CAS-code OPV from a semiconductor circuit and a control amplifier from a power supply circuit in SOI technology.

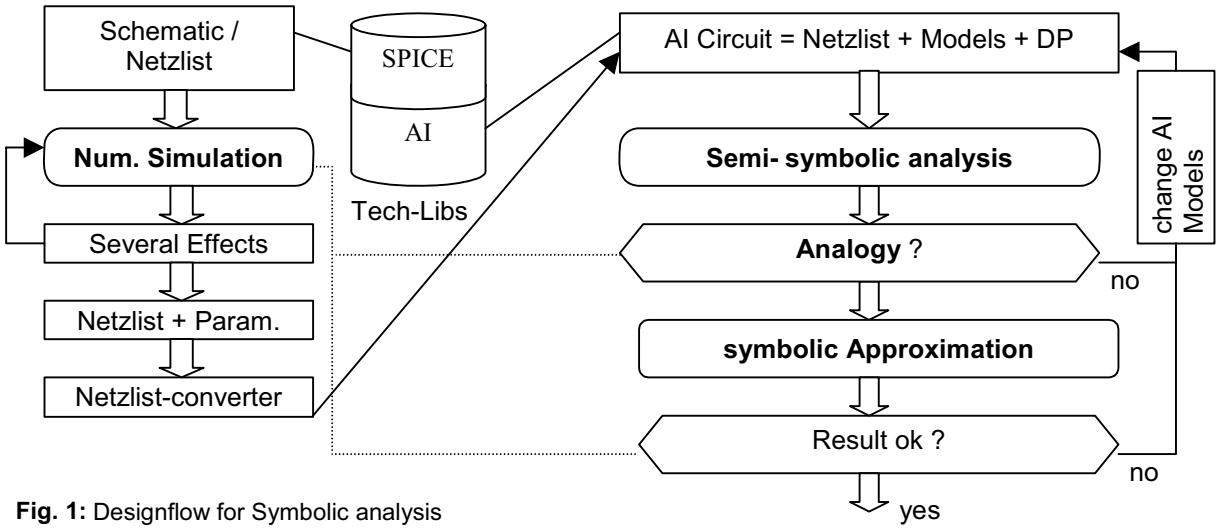

Fig. 1: Designflow for Symbolic analysis

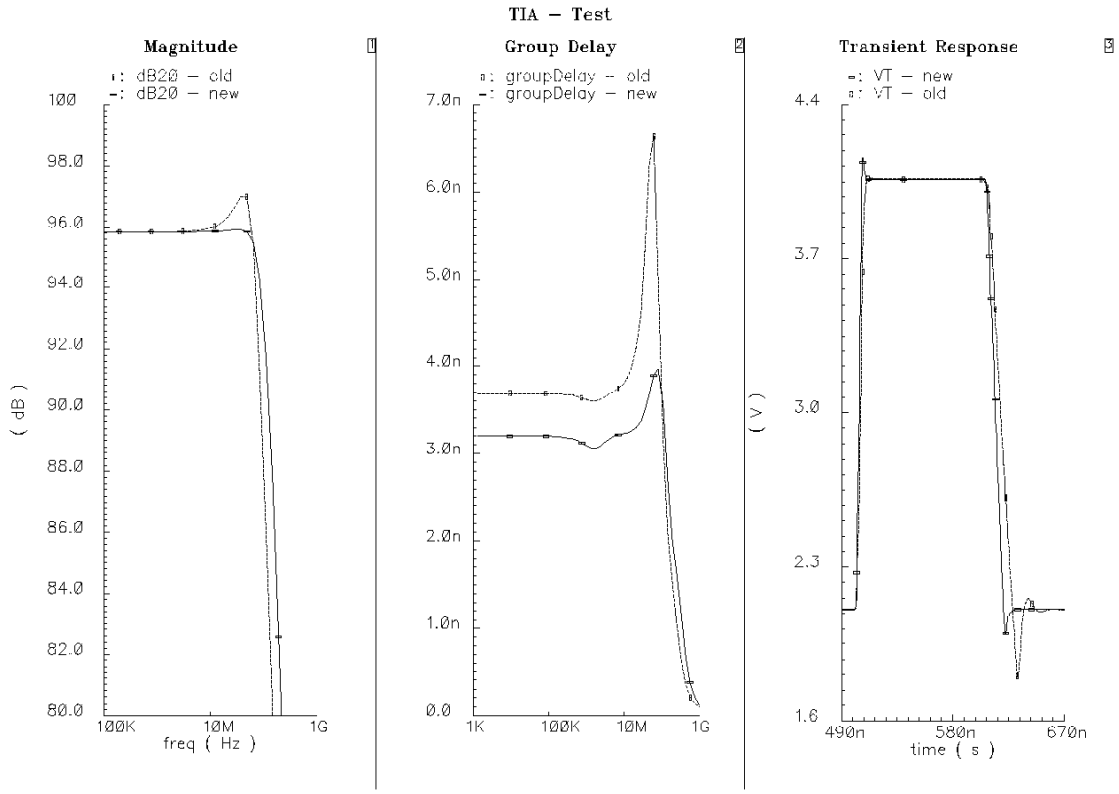

Fig. 2: Simulations results before and after Optimization

Outlook

Repeated iterations using conventional methods having been unsuccessful, the new procedure's excellent performance is demonstrated in these results. The intention is therefore to apply symbolic analysis and central design fairly comprehensively, in order to increase effectivity.

At present, symbolic analysis requires relatively intensive preparation before it can be applied. The Analog Insydes models have to be created for the relevant technology, the netlists out of SpectreS have to be adapted manually, and circuit elements have to be simplified.

Symbolic analysis is not a procedure that will display easily evaluated results at the touch of a button. It requires not only wide knowledge of circuit engineering but also a good deal of mathematical know-how, some of it specific to the application, to get the user from a netlist and the numerical simulation data to a qualitative evaluation. For this reason, symbolical analysis tends not to be used by IMMS circuit engineers in general, but to be offered by the section as a service, also provided to external partners.

The continuation of the *ANASTASIA* project includes plans to develop tools which can reduce the manual effort and enable symbolic analysis to be integrated into the design flow of IMMS and its industrial partners.

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Objective

The DVD Bluespot project is aimed at the development of optoelectronic sensors for the next generation of DVD drives, which will work with blue laser light. By transferring from red reading systems to blue, the recording density could be considerably improved, and thus the capacity of DVDs. A DVD recorded with red light can have 4.7 gigabytes and a DVD with blue light 27 GB.
The industrial partner in the project is MELEXIS GmbH (Erfurt).

Progress and status of research

Last year (2002) saw the development and manufacture of a single-channel version of the optical sensor. The considerations governing the design were:

- Need to design a system with high sensitivity (30 mV/µW) for blue light (λ = 405 nm) and thus with high transimpedance of the whole system (200 kΩ)
- Need for evaluation of photocurrents in 100 nA range
- Wide bandwidth (> 100 MHz) and high slew rate are necessary
- Low offset voltage and high linearity
- Need for a flexible design allowing transimpedance to be varied and amplification to be switched through a number of stages.

An amplification pattern with multiple stages was developed which amplifies in three stages the photocurrent generated by the photodiode- and convert it to a voltage. These three stages are

1. current amplifier
2. transimpedance amplifier
3. voltage amplifier.

The advantage of using this topology is that the amplification can be modified at any of the three stages. Each stage can be optimised for high speeds, which makes it possible to achieve very fast circuit with very high sensitivity. The approach also allows to exploit separate switching concepts for each stage, which allows to build a circuit with many degrees of freedom and adjustment of the sensor features to match the specific requirements and optical details of the exactly defined DVD pickup.

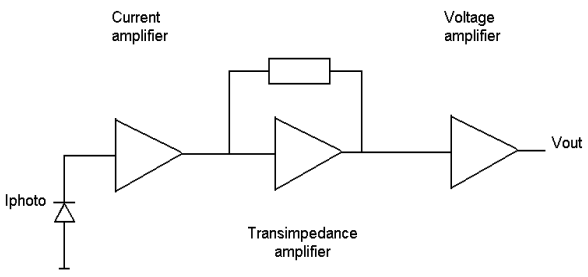

Fig. 1: Circuit diagram

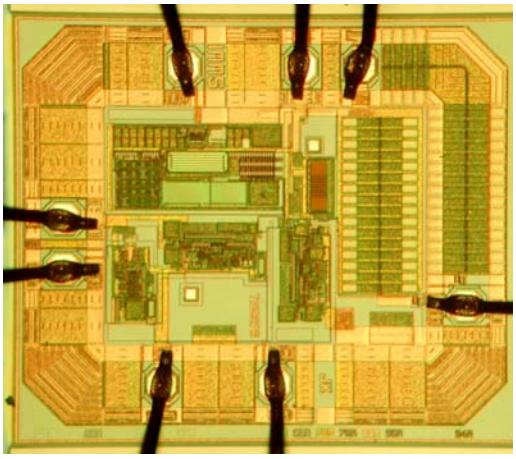

Fig. 2: Chip with single channel

The sensor can thus be employed in a variety of optical systems and could, for example, be adapted to manufacturers' optical DVD pickup specifications for read-write operation. It also permits the reflectivity of the DVD to be compensated.
The system as developed uses a special finger photodiode. The bandwidth achieved was in the 100 MHz range, with sensitivity of 30 mV/µW. Further optimisation of the system is planned.
In parallel to the above work, a specification has been prepared for a system with three-

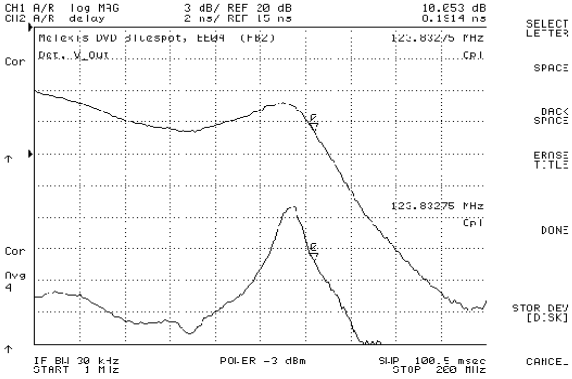

Fig. 3: AC simulation results

stage switching (the TH7525, see below), with a view to meet future demands for multi-channel DVD Blue systems.

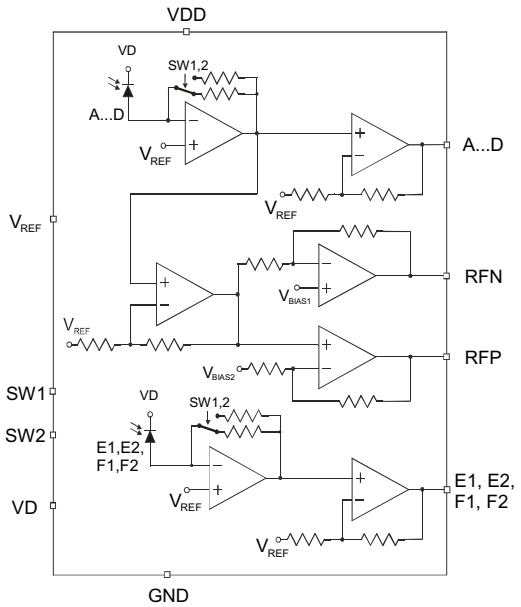

Fig. 4: TH7525

Outlook

Work continues, with the aim to develope a complete pickup with 8 channels (4 slow ones and 4 fast ones) all with three switching stages. The first engineering samples will be available by the end of 2003.

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Integrated optical receivers and transmitters for optical data transfer

Objective

The aim of the work being carried out in the Low Cost Data Comm project is the design of a reasonably priced optical data transfer system for use in industrial settings which require particularly fast and reliable data transmission. The system comprises the transmission fibre and the coupling module for the optical to electrical signal conversation. An optical beam divider in the link module sends the light from the fibre to the receiver and couples the light produced by the VCSEL diode into the same fibre. The integrated optical receiver, the VCSEL diode and the modulation circuit are all contained in the link module.
The part played by IMMS in the project is the design of the integrated circuits which control the VCSEL diode and the data receiver.

Progress and status of research

2002 saw the design of a start-up circuit for the intended VCSEL diodes (which have wavelengths of 635 nm or 850 nm). The driver will modulate a current of 20 mA (max.) if the bias current is not more than 12 mA. These two currents can be set by means of external voltages so that the power of the light to be sent on can be regulated. The data rate planned is 625 MB/s. The driver circuit has been designed to match these prescribed limits and is now being created. The block diagram for the VCSEL start-up circuit appears in Fig. 1. The

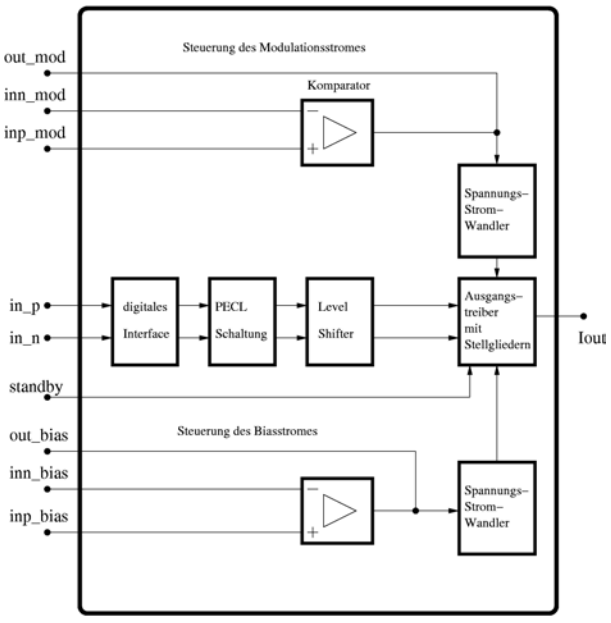

Fig. 1: Circuit diagram for the VCSEL driver

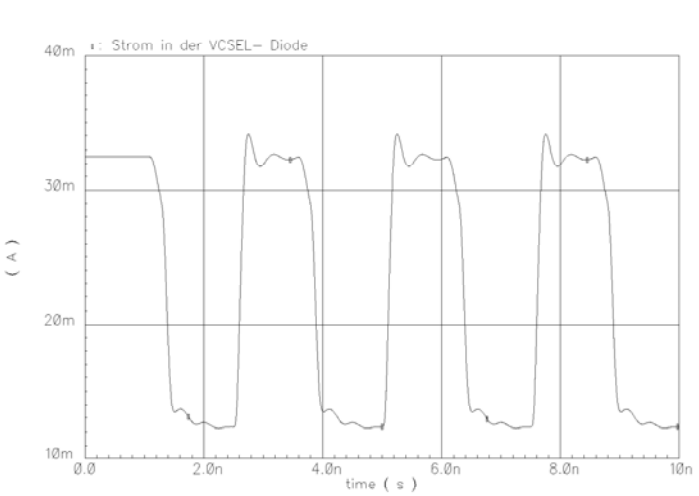

Fig. 2: Result of simulation of the VCSEL driver with a square input signal at 400 MHz

incoming differential signals are fed in at a PECL level. Standby input is available to permit the output current in the VCSEL diode to be completely switched off.
Figure 2 shows the simulation results for the circuit when the incoming signal is square and symmetrical at a frequency of 400 MHz.

Outlook

Design engineering of a data receiver is proceeding, to produce a functioning demonstration system for the physical transmission route. Once the VCSEL diode start-up circuit has been measured and characterised, a demonstrator is to be made for an optical data transfer route at 625 MB/s.

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Fully intergrated LC-VCO

Objective

The HF circuit design section is busy with, among other things, the development of circuits for applications in the licence-free 433 MHz, 868 MHz und 2.4 GHz ISM radio bands. A key component for high performance are oscillators which provide reference frequency. As the quality of integrated inductors has always been low and modelling difficult, completely integrated LC oscillators have rarely been used to date. The recent development of IC technologies and design tools has changed this situation. The use of fully integrated LC oscillators has now become possible.
They offer certain advantages over previous solutions:

- much lower phase noise than ring oscillators
- lower costs and better reproducibility than LC oscillators with external inductors

The LC-VCO designed in the present work is intended for use in a transmitter at 868 MHz. It will replace the ring oscillator used to date. As it has much lower phase noise, it is associated with considerably higher power output with no increase in outgoing interference.

Results

The LC-VCOs have been realised in a 0.6 µm BiCMOS technology. The integrated inductors have been developed and optimised at IMMS. It has become clear that the coils should be used differentially as the differential quality factor is about 20% higher. Various VCO topologies employing differential inductors have been investigated.
Two topologies were selected for detailed investigation and optimisation. Version A is a simple topology based on the Pierce oscillator circuit. Version B is a differential NIC circuit with common mode feedback to stabilise operating point. Version B achieves partly better parameters. However, due to its greater complexity deviations from the simulation are have to be expected.

	Version A	Version B
Current used	1,3mA	1,9mA
Tuning range V_t=0.5 V...2.0 V	25%	12%
Frequency deviation due to temperature and technology	20%	15%
Phase noise at 10kHz	<-78dBc/Hz	<-81dBc/Hz

Table 1: Simulation results

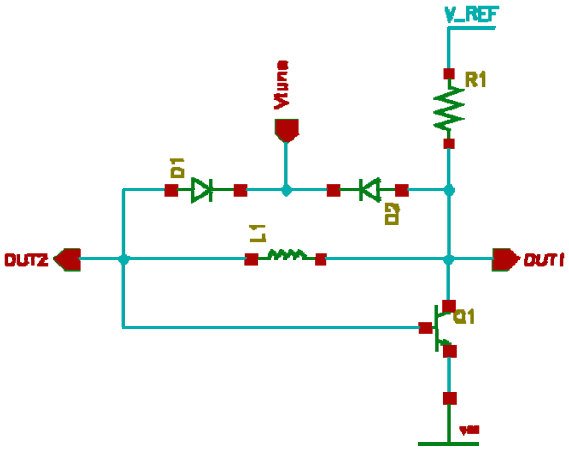

Fig. 1: Version A

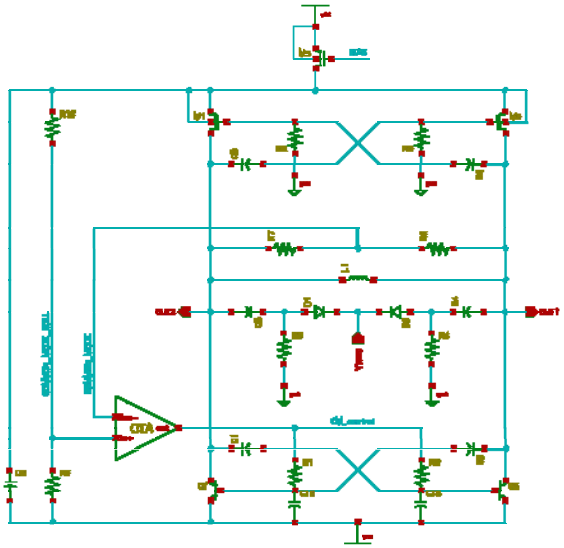

Fig. 2: Version B

Outlook

Both VCOs are going to be realised individually and in a transmitter on a test chip. This will permit the simulation results to be verified, and effects which cannot be simulated to be checked out.
The simulation results so far show that the tuning range is probably not adequate to compensate for the deviations due to temperature and process variations. In 2003, therefore, the investigation of local calibration techniques for LC-VCOs will be a focus of the work.

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Objective

Complexity in the field of micro-controlled actuator sensor systems, as in many other fields, is bound to increase in the future, throwing up the need for new methods and procedures in design. To avoid design faults, it will be necessary to verify the entire system on a single unified platform. The point of view of the software engineer must be taken into account just as much as that of the hardware developer. The SpeAC research project (Medea+ Project A508) has therefore been concerned with co-simulation of a graphic system description and a micro-processor simulator. The work is carried out jointly with Melexis GmbH, Erfurt.

Progress of Research

The tools available on the market for graphic system development were investigated, and Mathlab/Simulink by Mathworks selected. The command simulator used was the software simulator of Melexis' 16-bit micro-controller, MLX16.

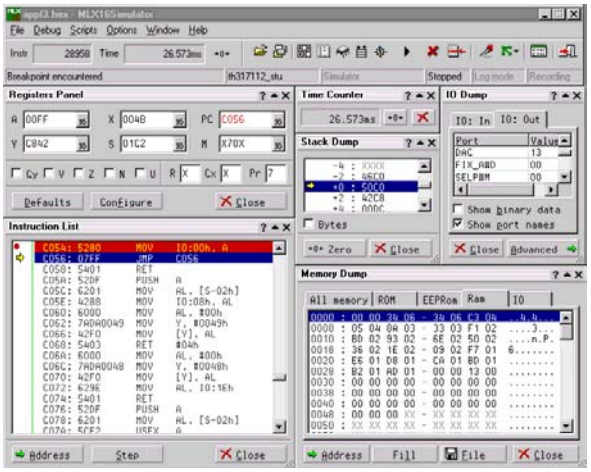

Fig. 1: MLX16 ISS screen

This ISS (Instruction Set Simulator) is equipped with a COM (Component Object Model) interface, which permits nearly all the functions of the ISS to be used as C++ function call-ups from outside. An S-function enables the ISS to be linked by this means into Simulink. The code used to do so is binary code compiled for Simulink.
The parameters to link the ISS into the Simulink environment can be set for inputs, outputs, and interrupt sources. A file is used to set the parameters. The control files for the simulation are generated from this with a graphic configuration tool. The timing is exactly synchronised between both programs. To achieve as high a rate of simulation as possible, data exchange only takes place when the processor is sending or calling up data used in the Simulink environment.

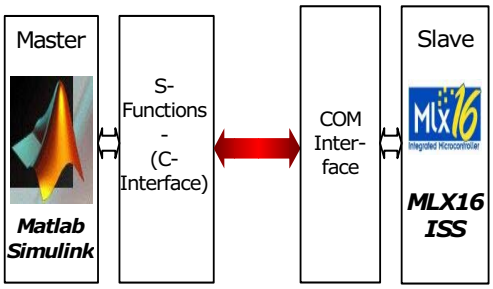

Fig. 2: Interface between ISS and Simulink

Pump control as example of use

State-of-the-art vehicles will soon have demand-oriented fuel pump control installed, replacing the present feedback systems. In the new systems, 3-phase BLDC (brushless DC) motors without any sensors will be used. These motors have the advantages of high energy efficiency and long lifetime as there are no friction points. However, their disadvantage is the complex start-up, which must take account of the current angle of rotation of the motor. This angle can be detected by analysing the induction voltage in the coil when no current is flowing. For this start-up procedure and other functions, a micro-controller which has made-to-measure integrated peripheral components is the solution. The application acts as control and monitoring system to the motor activity. Control circuits can thus be created as appropriate.
It has been shown within the project how such a complex system can be graphically modelled and, using the simulator link*, the application software can be simulated without modifications. Verification is simultaneous*. The motor start-up was checked out with the original software by way of example (see p..5).

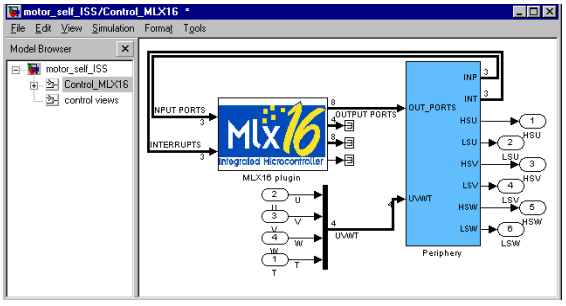

Fig. 3: Viewing ISS in Simulink

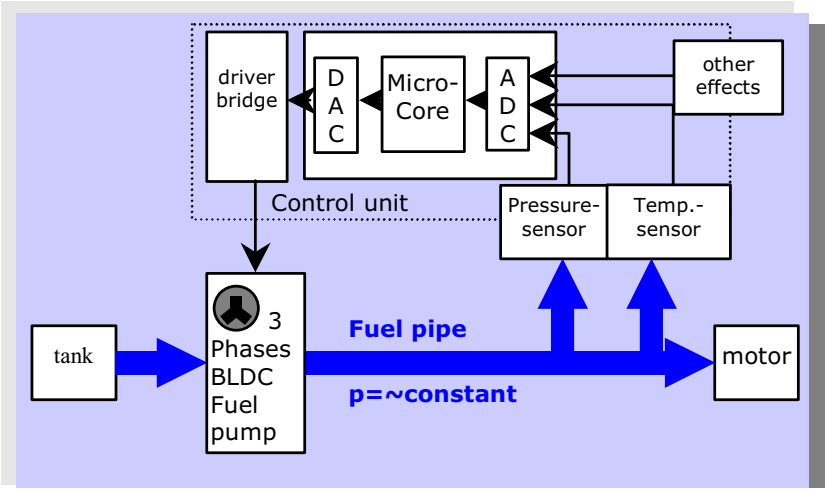

Fig. 4: Principle of control system for fuel pump

Outlook

At present it is the linking of the Melexis MLX4 simulator which is the focus of the work. In this case, the micro-controller is of the 4-bit dual or single task type. This simulator will be connected up similarly to the MLX16.
There are also plans to make the MLX16 work for SystemC™. In that case it is to be expected that the simulation rate will be even faster and there will be no dependence on the simulation software.

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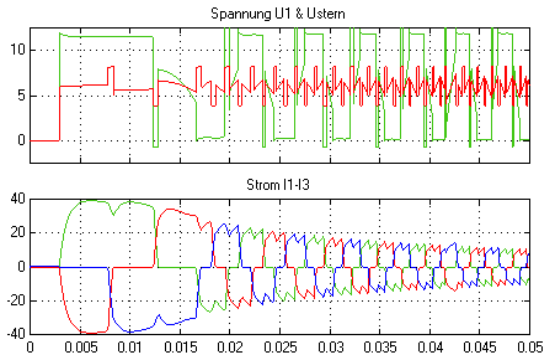

Fig. 5: Simulated motor start-up

Formal verification of mixed signal circuits

Objective

There is increasing use of integrated circuits in such critical safety situations as automobile manufacture. The highest possible quality of design is thus demanded along with the lowest possible price. The latter is not easy to achieve because of the increasing complexity of the circuits. The biggest problem at present is the heterogeneous structure of the circuits. On a single chip there will be digital blocks, power electronics and such analogue components as amplifiers and ADCs.
Unwieldy mixed-signal simulations have been the only means of verification to date for such circuits. However, in order to ensure correct functioning of a circuit in all conditions, many test patterns are necessary, even though they require too much simulation time. Even then not everything is covered by the testing.
Formal verification offers one way out of this situation in that it ensures that a circuit fulfils certain specifications by going through an exact mathematical proof.

Progress and status of research

Tools for formal verification are being developed and improved within the *VALSE** research project, and preparations are being made for their application. Infineon Technologies AG has created the toolbox for formal verification of digital systems named CVE (Circuit Verification Environment). The Gateprop tool in CVE is a model checker made available to the partners in the research project. At IMMS, Gateprop has been applied also to the verification of mixed-signal systems. This work has been shared with Melexis GmbH and involved replacing the analogue components with suitable digital models.

Model checking

Model checkers permit the properties of a digital system to be verified against a digital description of the behaviour (in VHDL or Verilog). The properties describe with mathematical exactitude the behaviour of the system requiring verification, and as such are capable of interpretation by computers. Gateprop can verify that the properties are fulfilled in every possible state of the system.
As Gateprop can, on principle, only verify digital circuits, direct verification of analogue components and how they function in conjunction with the digital modules is not possible. Up to now, it was necessary to rely on traditional mixed-signal simulation for mixed signal designs. The specification was converted into test patterns which were then verified by means of simulation against the netlist of the mixed signal circuit (see Fig 1 (a)).

Verifying analogue cells

Gateprop can, all the same, be used to verify the correct joint functioning of analogue and digital blocks if the relevant digital models are created for the analogue blocks. After the verification, these digital models must be replaced by the analogue circuits which have been verified by means of simulation.
To use the advantages of formal verification for mixed-signal designs, as well as digital set-ups, the specification of the system is first described in terms of properties (see Fig. 1 (b)). For the mixed-signal system which is to be verified, a purely digital behaviour description is produced, in which the analogue components of the system have been transformed into digital behaviour models. Gateprop is then used to verify the properties against the digitised system behaviour by

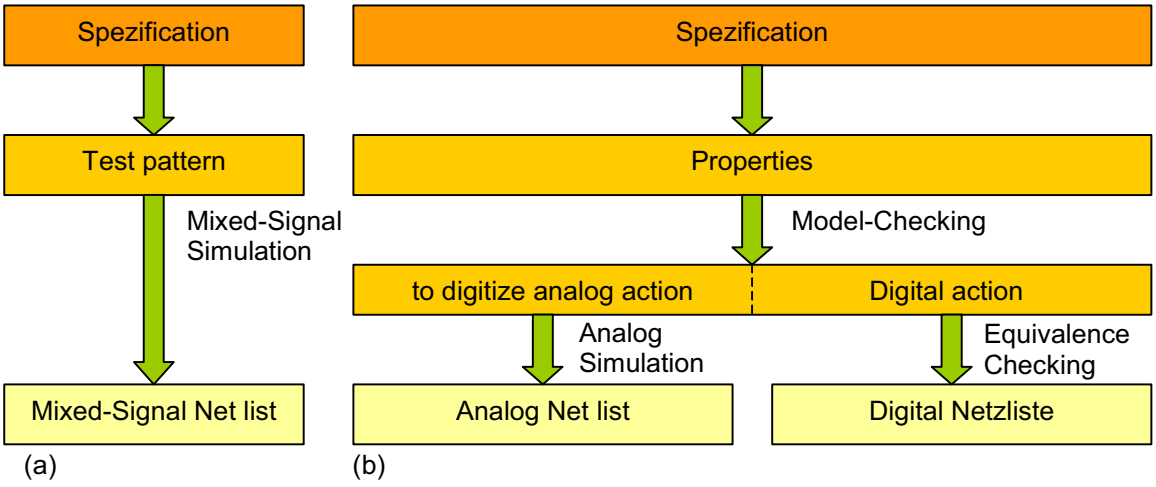

Fig. 1: Design flow for mixed-signal systems: (a) mixed-signal simulation (b) model checking.

means of model checking.
The digitised behaviour models of the analogue components have to be verified against the netlists of the analogue circuit by means of analogue simulation. The digital part can be verified against the digital netlist by means of equivalence checking. The advantage of this design flow is that unwieldy simulation is now not required at the system level, but only for the individual analogue components.
The analogue signals are represented as scaled integers. The word width of the integer signals is determined by the accuracy required in the analogue part. The function of the analogue blocks is now modelled by means of arithmetical operations with these integer signals. The verification model for an amplifier with amplification G is illustrated in Figure 2. The amplifier is replaced by a digital multiplication block.

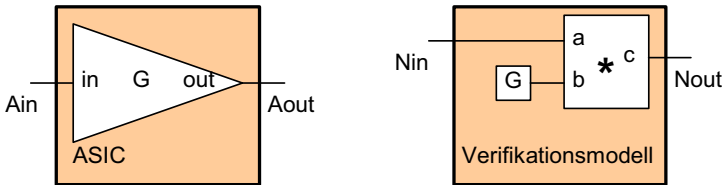

Fig. 2: Verifying analogue cells (a) amplifier (b) verification model of the amplifier.

Results

The verification methods developed were tested on a controller IC for an electric motor. The analogue part of the IC is an array of programmable amplifiers, analogue multiplexers and an analogue-digital converter. Among other things, the digital part contains counters for controlling timing and ROM for the configuration.
Gateprop enabled the behaviour of the circuit to be verified while taking account of the range of tolerance in the analogue components. Likewise, it was possible to verify the behaviour of the circuit when the analogue inputs are overdriven. The time taken to verify the analogue part was in a range of only a few seconds.
The method presented does have its limits if there are complicated mathematical dependences in the analogue part. If the characteristics are strongly non-linear, their digital models will be so complex that direct verification using toolboxes so far available still appears difficult. It is only possible to verify these analogue cells by means of simplified digital models.

Outlook

The present position is that analogue cells are being replaced manually by digital models, and this is, of course, a potential source of error. A library to produce the digital models for the analogue cells could be of assistance. Then the analogue cells could be automatically replaced by the digital models.
Projects planned for the future involve extending the use of Gateprop to processors with ROM control in order to verify these circuits in conjunction with the ROM contents.

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Objective

The performance of a printed circuit board (PCB) is determined on the one hand by the design of the circuit and on the other by the layout that proves possible on the board. The importance of layout applies particularly to the analogue and HF design. However, even in the digital circuit engineering task, which can easily involve switching frequencies of 100 MHz and pulse edges below 1 ns, it is no longer possible to look on the paths for the circuit tracks on a board as automatically ideal links.

Progress and status of research

The development of the board itself is a major step within the design flow. A circuit which is functional at the schematic level is not bound to turn out as a properly functional circuit on the finished board. Simulations tend not to pay sufficient attention to a number of parameters which have a strong influence on function. Circuit functioning can be adversely affected by:

- stray coupling or masking between circuit paths
- buffering, reflection and transit time on the paths
- parasitic capacity and inductance processed by wiring and components
- leads for ground connection or operating supply which are unfavourable.

The negative effect may be a tendency towards oscillations, poor selection or low sensitivity, distorted pulses or interference from irregular, intrusive pulses. How the board is laid out will also determine how much radiation of electromagnetic waves takes place, or the degree of sensitivity to incoming radiation. Suppression of radio and electromagnetic interference is required to achieve CE conformity and can only be achieved if the PCB is thoughtfully designed.

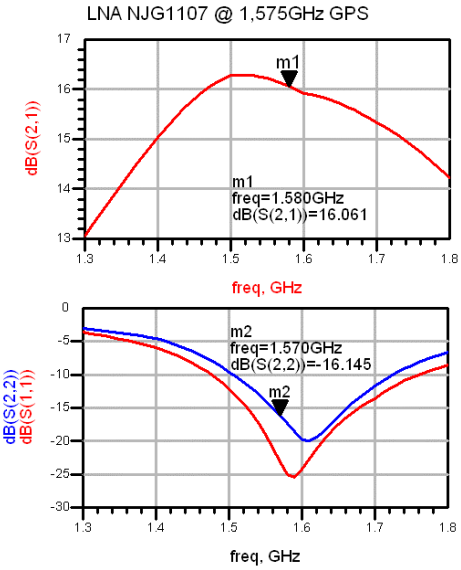

Fig. 2: amplification and adaptation of the LNA without SAW-filter

If a high degree of integration is planned – with few external components being necessary – circuit design is an easier task. On this basis, the SiRF GPS chipset is made up of two ICs, an analogue HF part and a digital part, and – depending on the application – requires by way of extra HF components only one active antenna, LNA* and a front-end filter. These deserve particular care if the GPS receiver is to be combined with a GSM module in a tiny space. The constraints mean finding the best compromise between noise-restricted sensitivity and large signal (IP3) stability. To find that compromise, data derived from simulation must be verified by actual measurement (see Fig.1). To achieve a functioning layout in ball-grid (BGA) casings which have 0.5 mm between the pins, a multi-layer board is essential. It is also possible to use buried vias or micro-vias placed directly into the pads, thus saving on routing levels. It is generally important to clarify the exact design rules with the manufacturer before the IC platen is out-sourced.

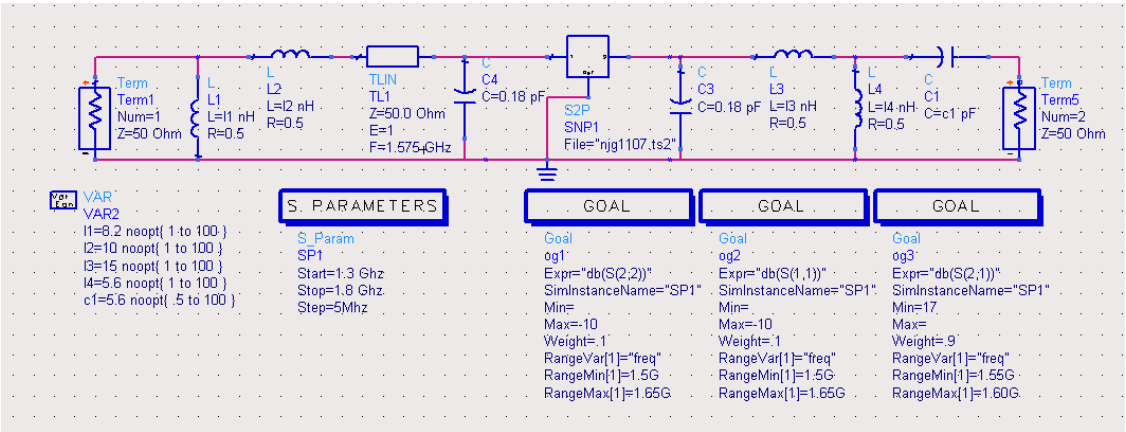

Fig. 1: simulation setup for GPS-LNA in ADS (Agilent)

Results

In a joint project with Falcom Communications GmbH of Langewiesen, various GPS receivers and GSM modules have been constructed separately and in combination, in all cases with major emphasis on the HF section of the GPS receiver.
A variety of MMICs were tested as pre-amplifiers (LNA). Their purpose was to compensate for the losses in the HF input wires and the front-end filter, and thus to reduce the noise figure for the whole system. The antennae used were either patch antennae or off-set active antennae.
The following parameters were set as the goal for the LNA design:

- Gain > 10 dB
- NF > 2 dB
- SWR < 2
- *Selection > 25 dB (at 900/1800 MHz)*

To achieve the parameters given in the technical data sheets for the MMICs, it is again necessary to select carefully, this time the passive components. In the case of the inductances it is particularly important to take care that the Q quality is high enough.
Another essential for the HF layout to be successful is that the link wires and transitions are impedance-controlled – i.e., the high frequency connections must be made with micro-strip or stripline which has a defined wave resistance.
Of the ICs investigated, MAX2641, NJG1103 and NJG1107, the circuit containing the NJG1107 yielded the best results (see Fig. 2). The data are given in Table 1, which also reveals that the target parameters were also achieved in the application which had an off-set active antenna with approx. 4 metres of RG-174 antenna wire.

Fig. 3: realised GPS/GSM-Board

Parameters	LNA only	Activeantenna
Amplification	16 dB	10 dB
Noise figure	1.3dB	1.7dB
SWR	1.7	1.7
Selection	>30dB	>30dB

Table 1: Parameters of the LNA with NJG1107

The lead-in wire to the active antenna has leakage of 6 dB, which is, however, only triggered by an increase in the noise figure for the whole system of 0.4 dB.

Applications

A range of GPS receivers has been developed as hardware for GPS. They are intended for integration into a dual-band GSM-GPS platform but can also be used as stand-alone modules (see Fig. 3).
To name certain examples, the JP2...JP5 class GPS modules are characterised by

- compact single board design (22x30mm)
- a 12-channel GPS receiver
- NMEA-0183, RTCM SC-104 and SiRF binary data format
- power management: trickle power mode
- excellent TTFF acquisition rate
- an integrated LNA
- GPS accuracy to below one metre

The JP3 board is a system offering the hardware base for compact, low-power, highly efficient OEM navigation or safety or monitoring products.

Services

IMMS can provide services in the following fields:

- Circuit design
- Design of PCBs
- Construction of trial boards / systems
- Descriptive analysis using measurement of DC and HF up to 50 GHz
- Consultancy and training

The engineers at IMMS have not only a wide variety of design and measurement tools at their disposal, but also the necessary know-how and experience to assist their industrial partners.

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Developing high-temperature circuits in SOI

Objective

The SOI circuit engineering section has been working on the following tasks in 2002:

- Development of analogue and digital IPs as library elements for X110 technology
- Further development of the CADENCE design kit for the X110 technology
- Design and layout of a 42 volt power supply (in the ANASTASIA+ EU project)
- Development of EEPROM and SRAM structures and of analogue sections of blocks, based on X110 SOI technology (in the ATHIS EU project).
- Design work for a preliminary exploration of an SOI-ASIC
- Modelling of TLP readings from ESD protection devices (in the ASDESE project)

In all these tasks, it was seen as valuable to ensure all the developments, structures and analogue blocks, were re-usable. The rest of this report presents one example of the section's work, that within the ATHIS project.

Progress and status of research

The ATHIS project began in April, 2002. Its full name is **A**dvanced **T**echniques for **HI**gh temperature **S**ystem-on-chip, and it has EU funding. The duration will be 42 months and IMMS is to be involved throughout. Other partners are institutions and companies in Belgium, Britain, Germany, Italy and Spain. The project is concerned with showing on a demonstration model that integrated systems for use in temperatures above 200 °C can function and be successfully tested.

The overall goal of ATHIS is to develop a complex ASIC for the automotive industry. It is to be used in controlling an actuator. The circuit must be able to function in the high temperatures (up to 200 °C) which arise cyclically in the vicinity of the engine.

For this reason, the ATHIS project decided to make use of a 1µm SOI technology.

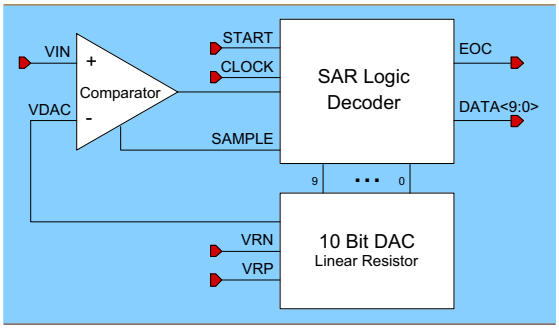

Fig. 1: AD converter circuit diagram

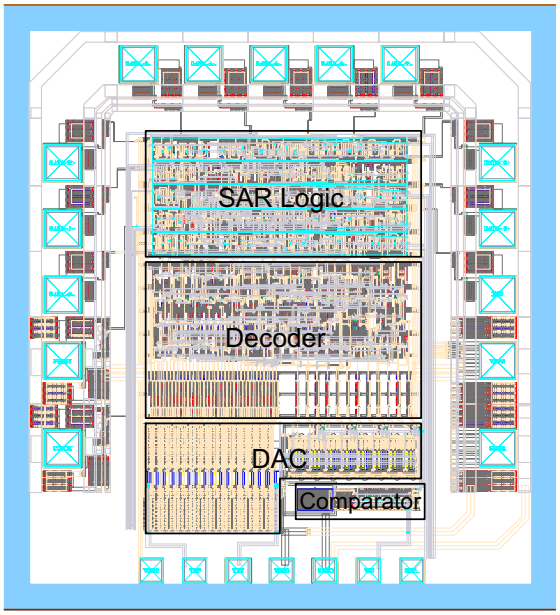

Fig. 2: AD converter Layout

The part to be played by the IMMS SOI circuit technology section is the development of the memory blocks (with volatile and non-volatile memory), and of the analogue IPs.

The non-volatile memory types considered were EEPROM, EPROM and ROM. New "single poly" cells were designed for EEPROM memory and their measurements taken. The EEPROM cells have a 4-volt programming window. It will be necessary to investigate these cells further in the next year, to try and reduce the programming voltage while receiving the same programming window. In parallel, EPROM cells and mask programmable ROM cells have been created and tested. The memory principle currently adopted for the non-volatile memory is a matter agreed by the various ATHIS partners. SRAM was the choice for volatile memory, and the first structures have already been designed and analysed. Different versions of memory have been installed into casings and have passed their function tests at ambient temperatures. The investigations at higher operating temperatures are planned for the second year of the project. The knowledge gained so far will mean that a redesign can take place so that the assembly will be capable of being fully integrated.

The first circuit designed which will be usable in the project is a 10-bit analogue-digital converter based on SAR (successive approximation register) logic for high temperature applications (up to 250 °C).

The principle of the ADC is shown in Figure 1. The procedure decided upon made it necessary to use a 10-bit digital to analogue converter which was designed in such a way that it

could also be made available within ATHIS as an individual IP.
The complete layout of the chip of the converter is shown in Figure 2. Its core layout has a surface area of approx. 0.86 mm². Readings

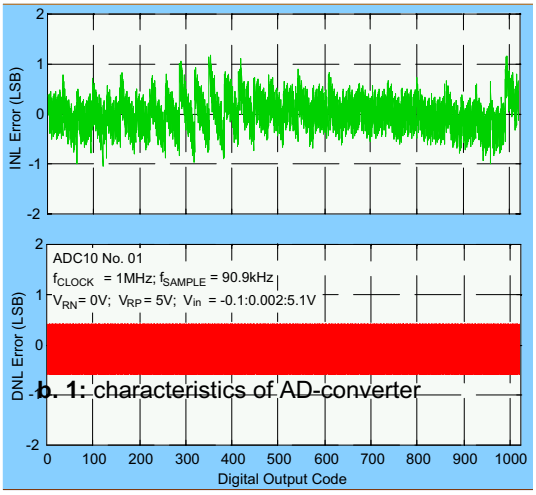

Fig. 3: Graphs of ADC measurements

taken at room temperature confirm that the ADC is fully functional.
The integral and differential non-linearity (INL and DNL) as measured are given in Figure 3. Table 1 shows the characteristic values of the converter.

Resolution	10 Bit
Integral non-linearity	± 1.0 LSB
Differential non-linearity	± 0.6 LSB
Current used (25°C, VRP-VRN=5V)	0.6 mA

Tab. 1: characteristics of AD-converter

The component was shown to function up to a frequency of more than 2 MHz (which is equivalent to a time for conversion of 2.5 µs or a conversion rate of 2 kilo-samples per second).
The remaining analogue cells designed for the project (operation amplifiers, band gaps, RC oscillators and charge pumps) all passed when tested on wafer for function at room temperature

Outlook

The work within the ATHIS project on the IPs will be continued until all have had their characteristics analysed for the temperature range from 25 to 225 °C. The integration of the analogue IPs with the digital sections to be designed by other partners will take place at IMMS. The associated verification will also be carried out.

In the ANASTASIA+ project, the step-down control and the linear control which have so far been realised as separate blocks will be joined together into one 42-volt power supply block. The investigation of the circuits with tools to help in centring the design (WICKET) and investigating stability (AnalogInsydes) will receive priority.

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Analysis and Testing

The Analysis and Testing department has built on the success of previous years, continuing its research and development in the analysing of noise and high frequency parameters in components operating in the 300 kHz to 50 GHz range as planned. The software for the analysis system represents the state of the art and the continuous refinements to the calibration routines which have been made mean that the measurement accuracy achieved matches the ever more stringent demands of the semiconductor industry. The high performance of the IMMS analytic methods was demonstrated at numerous conferences and workshops in 2002. Individual components continued to be tested, but, also, the analysis equipment has been expanded to meet the need for characterisation and testing of complex devices, for example RF-ASICs (see p. 42). A particular challenge that had to be met for this was the designing of testboards for these ASICs. In the solving of the complex wiring problems for mixed digital and high frequency systems, the experience gained over what was by then two years with the design of layouts for GPS and GSM systems (see p. 36) proved very useful.

To represent the very many digital and mixed signal testing projects carried out as services to other IMMS sections and to external industrial partners, the FUSE project (see p. 46) and the Q device can be mentioned. Industrial companies are taking more and more interest in all the initial work being done on methodology and hardware for mixed-signal testing. This preparatory work includes, among other things, extension of the temperature range under which devices are tested, with the purpose of meeting the ever more demanding specifications of the automotive industry.

In parallel with the activities in the Microelectronic Circuits section, a universal mixed signal testing station has been constructed which is particularly geared to precise analysis of analogue-digital and digital-analogue conversion systems. The resolution and the dynamic features of the analytic techniques which it combines are those demanded by converters built to the latest principles.

The department has not only worked on testing and measurement but, within the section addressing problems in circuit engineering, has been concerned with power electronics. Here the focus has been on dimmable electronic ballast devices for fluorescent lighting, and on battery management for lithium ion or lithium polymer batteries.

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Testing for SOI projects

Objective

IMMS has, for several years, been working with X-FAB Semiconductor Foundries AG, Erfurt, on SOI technology and SOI circuits. Verification and characterisation have taken place at IMMS on a great number of test circuit structures, such as transistors, digital cells, I/O cells, memories, Q devices and Hall sensor elements. The emphasis this year has been on testing, for the Q device and for the memories.

Progress and status of research

After the good experience with the verification of the basic digital SOI cells and the test structure for the XF20189.1 circuit, X-FAB Semiconductor Foundries AG Erfurt asked IMMS to do the characterisation for the XF20208.1 Q device.
There are six different I/O cells in a* Q device: a standard input cell, an input with Schmitt

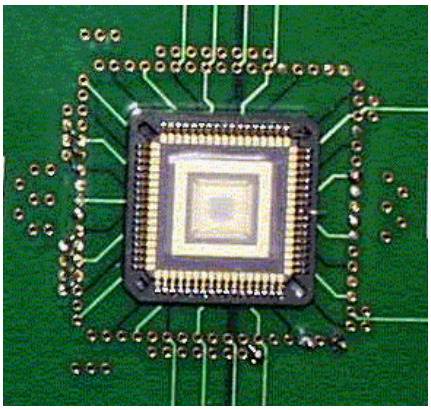

Fig. 1: XF20208.1 Q-Device

trigger, an input with pull-up, an input with pull-down, and two output cells with different driver capabilities. It also contains about 40 digital cells such as inverters, buffers, (N)ANDs, (N)ORs, EX(N)ORs and multiplexers. The XM20208.1 SOI Q device is in 10 blocks, which in turn are divided up into sub-blocks containing elements of the digital library. Each sub-block contains individual gates and chains of gates and provides four functions: logic, delay chain, ring oscillator and time pulse.
The project has included working out the test specification, developing the load board and adapting it for the test system, and converting the test patterns from the design. The HP82000 IC evaluation test system was used as the basis for the investigations, and external analysers were linked into it for dynamic measuring purposes. The software for testing was implemented in HP-VEE* and C programs. To enable the test report to be automatically generated, it was again HP VEE programs which were used to process the analytic values and transfer them into Excel spreadsheets. Characterisation was carried out at three temperatures: 25 °C, 70 °C and 125 °C.
The project ran from April to May 2002, in association with X-FAB Semiconductor Foundries AG's Design Department in Erfurt.
Verification work on single and dual port RAMs with different storage capacities was also carried out over the year at IMMS within the ”ATHIS” ASEDA research project.
A student from the university of applied science at Jena devoted his engineering placement to the on-wafer verification of a controller as component of the RAMs.

Outlook

A contract has been signed with X-FAB Semiconductor Foundries AG Erfurt for 2003, by which the SOI analogue library is to be characterised. Also, the analysis procedure is to be taken up to the 210 °C temperature range. Verification of a new dual port and single port RAM is planned for the start of the new year in the ATHIS project.

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Test environment for high frequency ICs

Objective

For standard ICs it goes without saying that all ICs are tested on wafer before they receive a package. For special, high frequency, ASICs made to the customer's requirements, it is not economic to test the entire functionality on wafer as they are made in such volumes.
Even testing RF ICs in SMD packages is no small matter, for, to function correctly, they require to be connected to the application circuit as a matter of course, and a standard test socket has parasitic elements which will definitively modify the function of the circuit.
The problem thus arises of how to construct a test environment that will enable the functions of RF ICs to be tested – a combination of some sort of IC tester and RF analytic equipment suitable for small series.

Progress and status of research

To attach the circuit to be analysed to the tester, a specialised evaluation or load board is necessary. The first question to settle is the contact between the IC and the board. Commercially available RF test fixtures (as used on the mass production scene) are simply too expensive to use on short runs.
The parasitics produced by an IC socket need to be kept as low as possible. But this means very short connections as the RF-critical components must be placed as close as possible to the IC.

A solution has been found to the contact problem – with the following positive features:

- simple, manual IC changing
- will use a normal SMD footprint
- external components up to 1.5 mm high directly attached to the IC are possible
- same RF layout with and without socket
- exchangeable insert for different casings
- re-usable IC socket
- socket variants with different layouts for quick change of ICs and simple mechanics
- moderate cost.

The lifetime of the socket is basically determined by the quality of the board, which should be surface-treated with hard gold.
The keepout areas used by the socket are not in direct proximity to the IC, which means that the design rules given in the actual application can be followed. Components which determine frequency can be laid out directly at the IC pins.
The evaluation board is connected to the IC tester by means of high frequency and DC wires or a circuit matrix. The parameter tests listed in the device test specification can thus run automatically with computer control for a whole IC, and the relevant test protocols also automatically produced.

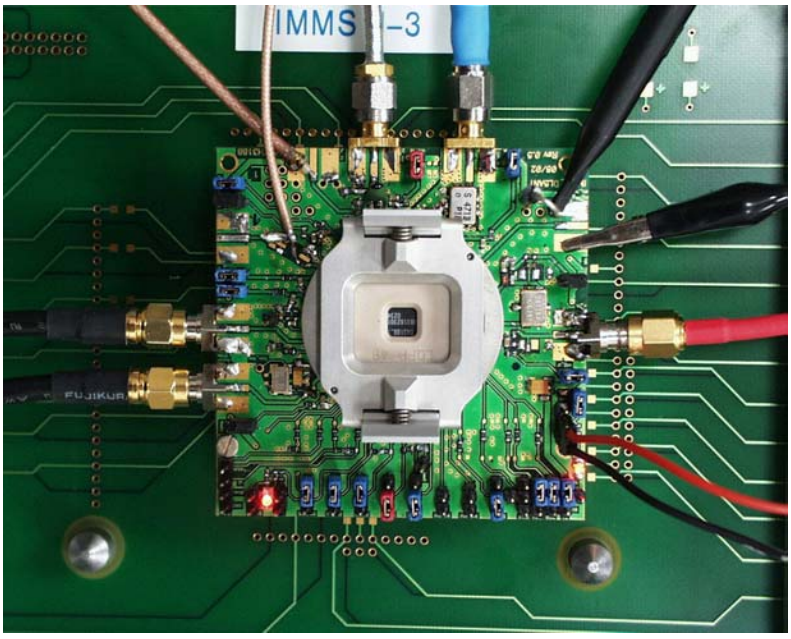

Fig. 1: Evaluation board on the HP82000 tester

Results

The RF-IC TH3188 was evaluated in cooperation with Melexis GmbH of Erfurt. This IC was made to the customer's requirements and operates at 470 and 940 MHz. It comprises a sender, a receiver, an SPI, an ADC and a controller, and is laid out for frequency and IQ modulation.
An evaluation board was designed for the triple purpose of optimising the circuit, analysing it and acting as a reference design (see Fig. 1).
HPVee is used to control the tester using a HPIB(IEC488) bus. The following external analytic devices may be attached:

- an ESA-E4404 spectral analyser up to 6 GHz
- an ESG-D4432 high frequency generator up to 3 GHz
- an SMIQ06B IQ signal generator up to 6 GHz with an ARB waveform generator and the option of analysing the bit error rate.
- a ZVRE network analyser up to 4 GHz with a time-domain option
- an oscilloscope
- HP6626 power supply

An RF circuit matrix is used to switch between analytic devices, and it must be appropriate to the frequency range used and the speed of measurement required. Special high frequency relays are used to ensure this.
Figure 2 reveals a possible set-up as used in the laboratory.

Outlook

Now that experience has been gained on high frequency ICs up to 1 GHz, more test environments are to be established. Besides putting test specifications into actual practise, ways are to be found of carrying out characterisation and testing of small numbers of ICs in the frequency range up to 6 GHz.
There is also the intention of making the testing procedures portable for use in other test systems.

Services

IMMS can provide services in the following fields:

- development of testing schemes
- design of evaluation boards
- IC testing (both DC and RF)
- characterisation of up to 50 components
- consultancy and training.

The engineers at IMMS have not only a wide variety of design and measurement tools available to assist their industrial partners, but also the necessary know-how and experience.

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Fig. 2: Analytic equipment as configured in the laboratory

Techniques for the characterisation of fuses which use 1.0 µm technologies and the optimisation of their programming

Objective

In 2002, X-FAB Semiconductor Foundries AG in Erfurt again asked IMMS to investigate the programming of fuses. The experience of the previous year proved valuable, the test hardware and test card being used again.

Progress and status of research

The fuses act to keep a circuit tuned at the wafer level. With this type of fuse and the right electronic analyser, it is possible to meet higher accuracy specifications for analogue and mixed signal circuit segments without specialised equipment.
The programming can change the fuse resistance from a few hundred ohms to a range in the thousands. Examples of where these fuses can be applied are automotive and communications electronics.
They are an element of design kits for semiconductor foundries. The outcomes from IMMS' investigations are being used in X-FAB Semiconductor Foundries AG's design kit for XC10 technology.

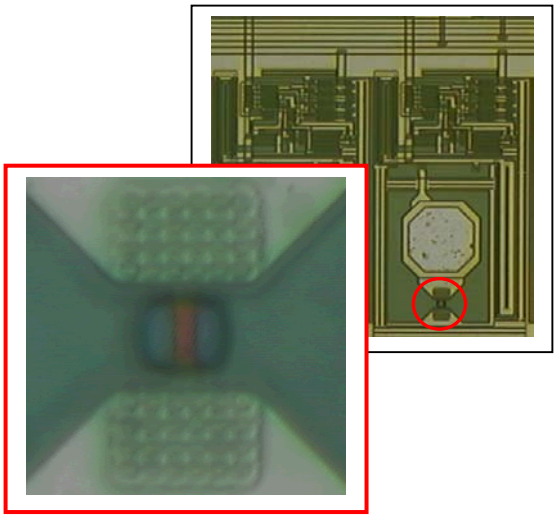

Fig. 1: Chip photograph of the fuses and one version of layout (enlarged)

Figure 1 shows an excerpt from the circuit structure and the fuses before they have been programmed. The chip photos were achieved in close co-operation with the Technische Universität Ilmenau's ZMN (Centre for Micro- and Nanotechnologies).
The project required the investigation of 48 fuse options. These involved eight different layouts, three thicknesses for the oxide layer and two types of passivation. The current-voltage characteristic for all these variants and a large number of actual fuses was recorded.

The analysis was carried out for both the U force and the I force programming modes. The resistance of the fuses before and after programming was also recorded at the same time, as were the parameters for the test structure. The characteristic curve (I against U) for a fuse in the U force mode is shown in Figure 2, in which the characteristic for 24 fuses of one type are superimposed on one another.
The analytic technology used for the characterisation was IMMS' IC evaluation system known as the HP82000. HP-VEE was used to implement the software. The programs were optimised and extended so as to be capable of analysing the readings taken. The measurements for characterisation, the programming of the chips for the Q devices, and the interval

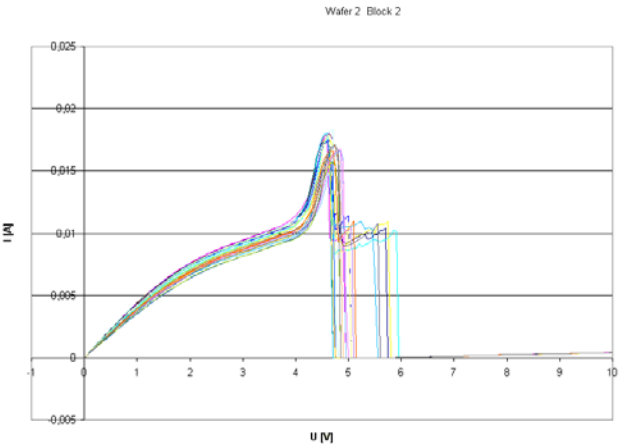

Fig. 2: I / U diagram of a Fuse variant, U-Force

measurements in the course of the life test were all carried out in full at IMMS.

Outlook

The test report on the characterisation was submitted in December 2002. The next stage is the selection of the fuse variants to be included in the design kit. Wafers will be programmed and constructed for the chosen fuses in the coming year. The components known as Q devices will undergo the 1000 hours' test and on that will be based the evaluation of the reliability of the programming that has taken place.

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Membership of Professional Associations and Working Parties

- **AMA Fachverband für Sensorik e.V.** - *Fachausschuss „Optische Sensorik“*
- **American Chamber of Commerce**
- **AZT e.V.** - *Automobilezulieferer Thüringen e.V.*
- **DFAM -** *Deutsche Forschungsgesellschaft für die Anwendung der Mikroelektronik e.V.*
- **DFN**
- **EIBA -** *EUROPEAN INSTALLATION BUS ASSOCIATION*
- **EUROPRACTICE**
- **Facharbeitsgruppe Mikrotechnik Thüringen (TMWAI-STIFT)**
- **Fraunhofer Gesellschaft / IOF Jena**
- **Mitglied Leitungsgremium der GI/GMM/ITG-Kooperationsgemeinschaft "Rechnergestützter Schaltungs- und Systementwurf (RSS)"** (Fachausschuß 3.5 der GI, Fachbereich 8 der GMM, Fachausschuß 5.2 der ITG)
- **GI/GMM/ITG-Kooperationsgemeinschaft "Rechnergestützter Schaltungs- und Systementwurf (RSS)"** Fachgruppe 1 "Allgemeine Methodik und Unterstützung von Entwurfsprozessen für Schaltungen und Systeme"; Fachgruppe 2 "Entwurf von analogen Schaltungen"
- **GMM –** Beirat
- **GNT -** *Gesellschaft zur Förderung neuer Technologien Thüringen e.V*
- **IEEE -** Circuit and Systems Society; Electron Devices Society; Solid-State Circuits Society
- **InnoRegio Südthüringen e.V.**
- **ITG-Arbeitskreis** "Zusammenarbeit Industrie und Hochschulen"
- **ITG Fachgruppe** "CAD für den Analogschaltentwurf"
- **Jury des BMWi zum Initiativprogramm “Zukunftstechnologien für kleine und mittlere Unternehmen”** - ZUTECH 1999 – 31.7.2003
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- **Programmkomitee Technologiesymposium MTT 2002** (Mikrotechnik Thüringen)
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- **USB - Implementer Forum**
- **VDE / VDI Fachgesellschaften ITG, EKV und GMM**
- **VDE / VDI -** Arbeitskreis „Mikrotechnik Thüringen“
- **VDMA -** Arbeitskreis "Nutzergruppe Mikrosystemtechnik"
- **VSIA -** *VITAL SOCKET INTERFACE ALLIANCE*

Papers and Publications

publications, lectures:

- Zellmann J., Czerner F.: **"A methodology for high-level design of machine vision systems using SystemC"**
  03/02; Paris, SNUG 2002
- Lang, Ch.: **„Verifikation von Mixed-Signal-Schaltungen im Automobilbau"**; 03/02; DASS`2002; Dresden
- Bieske B.: **„Empfänger-Chip-Entwurf für das 868-MHz-Band"**
  03/02; Fachzeitschrift „Elektronik Wireless", S. 75f
- Richter, St.; Göttlich W.; Dr. Nuernbergk, D.; Dr. Nakov, V.; Bormann S.: **„Hitzefest - Design von Mixed-Signal-Hochtemperatur-Ics"**
  03/02; Fachzeitschrift „Design & Elektronik", S. 56f
- Dr. Sinn, W.: **„Mobile Kommunikation - Wertschöpfung, Technologien, neue Dienste"**
  03/02; Betriebswirtschaftlichen Verlag Dr. Th. Gabler GmbH
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  04/02; Düsseldorf, Euroforum „Fachkonferenz für die Automobilindustrie"
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  Beckmann/Meister/ Heiden/Erb (Hrsg.): Technische Systeme für Biotechnologie und Umwelt - Biosensorik und Zellkulturtechnik; in: Initiativen zum Umweltschutz, Band 41, ISBN 3 503 06645 4; S. 203-213, Erich-Schmidt-Verlag, Berlin, 2002
- Prof. Scarbata, G.: **„Forschungs- und Entwicklungskompetenzen des IMMS gGmbH"**
  05/02; Erfurt, „4. Fachmesse und Technologiesymposium für Innovationen in der Mikrotechnik" (MTT) 2002
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  05/02; Erfurt, „4. Fachmesse und Technologiesymposium für Innovationen in der Mikrotechnik" (MTT) 2002
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  05/02; Bremen, Analog 2002
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  06/02; St. Petersburg, Russia, 26.-28. Juni, IEEE Conference for Circuits and Systems for Communications
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  Tagungsband zum 47. Internationalen Wissenschaftliches Kolloquium "Maschinenbau und Nanotechnik - Hochtechnologien des 21. Jahrhunderts" der Technische Universität Ilmenau, 23.-26. September 2002; S. 43f, ISSN 0943-7207, UB der TU Ilmenau, 2002
- Dr. Schäffel, Ch.; Katzschmann, M.; Mohr, U.; Whittingham, J.; Michael, St.: **„Modellierung und Simulation von Magnetlagern für hochdrehende Radialverdichter"**
  Tagungsband zum 47. Internationalen Wissenschaftliches Kolloquium "Maschinenbau und Nanotechnik - Hochtechnologien des 21. Jahrhunderts" der Technische Universität Ilmenau, 23.-26. September 2002; S. , ISSN 0943-7207, UB der TU Ilmenau, 2002

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  10/02; Stresa (CZ), 6th European SystemC Users Group Meeting
- Dr. Töpfer, H.: **„Design of HTS SFQ Circuits"**
  11/02; Yokohama (Japan), 15th International Symposium on Superconductivity
- Dr. Töpfer, H.: **„HTS SFQ Circuits Design"**
- 11/02; Tokyo (Japan), Vortrag am Hitachi Central Research Laboratory
- Dr. Schröder, Ch., Pietruski, J, Peukert, R.: **„Echtzeitsteuerung für mechatronische Systeme"**
  11/2002; Fachzeitschrift „Embedded Engineering", S. 28f
- Hauer, H.; Lang, Ch.: **„Intelligente Sensorsysteme"**
  11/02; Fachzeitschrift „Elektronik Embedded Systeme", S. 46f
- Dr. Stieler, W.; Dr. Töpfer, H.: **„Coole Visionen – Supraleitende Computer in greifbarer Nähe"**
  25/2002; Fachzeitschrift „c't", S. 170f
- Bieske, B.: **„Designmethodik für Low Power Kommunikationsschaltkreise"**
  12/02; Frankfurt/Oder, Kolloquium "Neue IC-Design-Techniken"; GFWW/IHP

general publications / research reports:

- Kindt, R.: **„Anastasia WP2 (work package 2) meeting"**
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- Mollenhauer, O.; Dr. Spiller, F.; Reuter, F.; Wehrsdorfer, E.; Ahmed, I.; Dr. Scherge, M., Hild, W.:
  Abschlußbericht zum Verbundprojekt „Präzisionsantriebe unter erschwerten Einsatzbedingungen"
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  04/02; TU München, 4. Workshop „Analogschaltungen 2002"
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- Mollenhauer, O.; Dr. Spiller, F.; Schilling, P.; Frenzel, G.; Prof. Höhne, G.; Prof. Hülsenberg, D.; Prof. Schäfer, J.; Prof. Kallenbach, E. u.a.:
  Abschlußbericht zum Verbundprojekt „Fabrikation von Mikro-Elektro-Mechanischen Systemen (MEMS-Fab)"
  Thüringer Ministerium für Wissenschaft, Forschung und Kunst; Förderkennzeichen B 609-98037; Ilmenau, 2002
- Geyer, H.: **„Durchgängiger modellbasierter Softwareentwurf für Kfz-Steuergeräte"**
  09/02; TU Ilmenau, Workshop „x-by-wire Technologien für Kraftfahrzeuge - eine Herausforderung für die Ingenieure der Zukunft"
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  06. November 2002; Erfurt, Workshop „Embedded Mixed Signal Systems“
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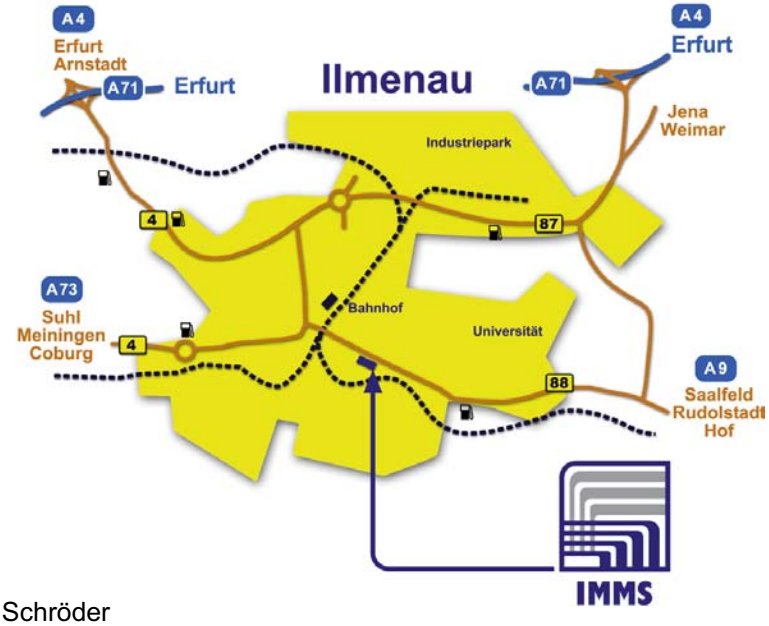

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