Annual Report

IMMS gGmbH

2001

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IMMS vis à vis Industry

IMMS sees itself as a bridge-builder: from the academic principles and theories underlying new procedures and processes (whether in the physical or technical sphere), to the good practical purpose they might serve in industry. Our aim is to enable our industrial partners to take the applications we design and to transfer them, without prohibitive cost, into new products. in which the innovation element will be either huge improvement or totally new features.

We are thus a node in networks formed by research establishments from a range of disciplines working together with equally varied industrial users. These networks linking research establishments and industry are meshed together particularly closely in Thüringen.

Small and medium-sized enterprises (SMEs) always find that IMMS is a most valuable, responsive and reliable partner, closing the gap for them between state-of-the-art science and the development of the new technological product. IMMS has built up Departments which enable it strategically to match competence in a subject to market demand. It foresees R and D needs and rapidly brings to bear on them knowledge and methods, devices and equipment, all geared to applications of practical use.

The Institute's development has followed a continuous progression since its founding.

Evidence of the progress is to be seen in the steady staff increase and in the way both the tools we use and the infrastructure we have to call on have been expanded and modernised. This is true of both our sites, in Erfurt as in Ilmenau.

Our work can be seen as output of the following:

- research and development services
- highly qualified engineering specialists
- the making available of state-of-the-art technical equipment
- the training of staff to think in terms of commercial use, and to work accordingly
- the encouragement of innovative product development by local industry.

The majority of this output benefits small and medium-sized enterprises in Thüringen. The map alongside is an indication of how active IMMS is in co-operating with project partners in Thüringen. It is a fair assumption that the Institute has contact with all firms in Thüringen involved in technological product development. It has, moreover, been IMMS' policy since 2001 to forge strategic alliances with innovative companies, at least those with a production site in Thüringen.

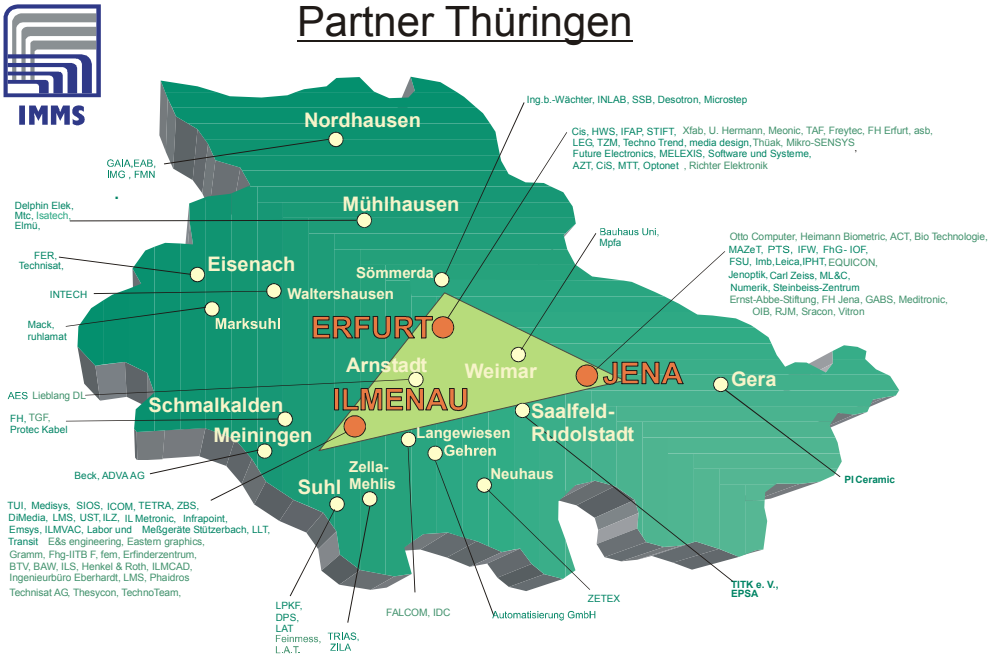


Fig. 1.: IMMS' Thüringen partnerships

As is convincingly shown by fig. 2, the research partners served by IMMS are, indeed, mainly Thüringen companies. There are, of course, additional research links with many others of the federal German Länder, and there are some international projects involving Austria, Switzerland, the Netherlands, Japan and the USA.

Recent years have seen changes in the industrial scene in Thüringen itself. Companies which were still small or medium-sized in 1998 are now, in many cases, large concerns because of mergers. The models for co-operation thus have to be organised flexibly to mirror the changes.

This background probably explains the fact that, although the number of project partners and even of projects has not significantly increased, the Institute's income from industrial

commissions has risen considerably. Industry's

interest in making use of research results to introduce new products to the market has palpably and significantly expanded.
The projects in which research has been done by IMMS to commission have become ever larger. We are now involved in a higher number of large-scale projects. This fact correlates with our experience of the vast amount of time and energy which must be invested in order to pursue an idea from applied research to a prototype which will be the preliminary to production.
Outline agreements are in place with a number of Thüringen companies to enable the latter to make comprehensive use of research results in the strategic development of prototypes. In addition, outright bilateral cooperation contracts with similar objectives exist.
These partnerships helped to establish the conditions for creating some absolutely new product lines which are also being actively and successfully marketed on the international scene with IMMS support.
In addition, IMMS is working with a number of industrial companies on joint projects and research commissions.

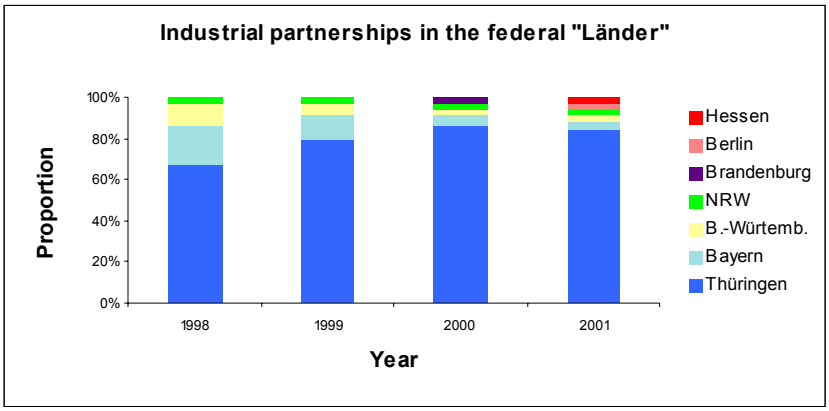


Fig. 2: Industrial partnerships in the federal "Länder"

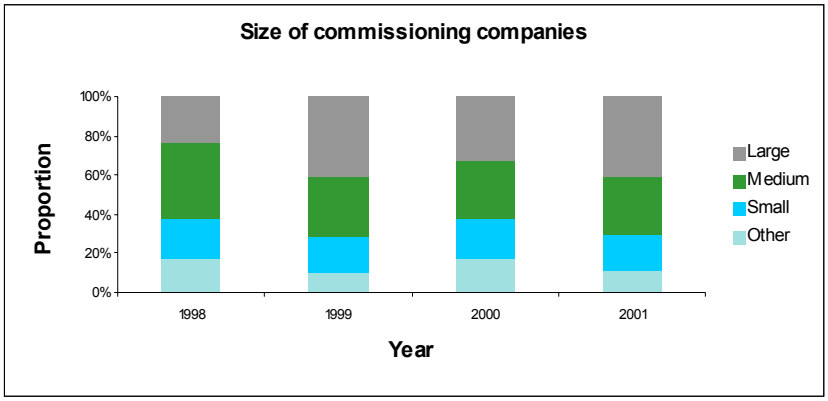


Fig. 3: Size of commissioning companies

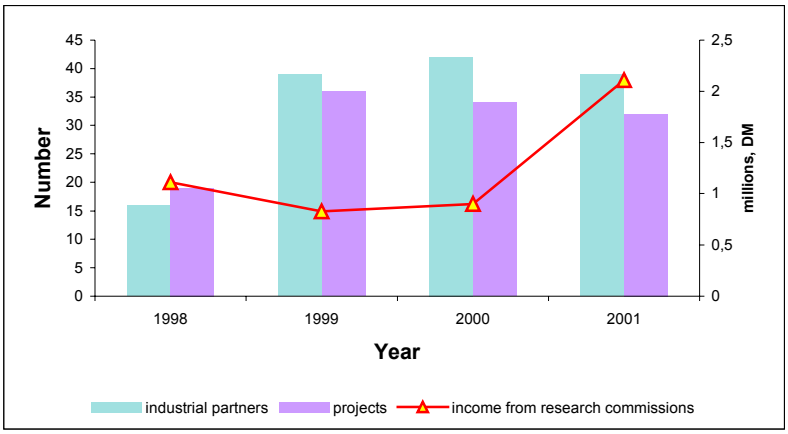


Fig. 4: Income from research commissions

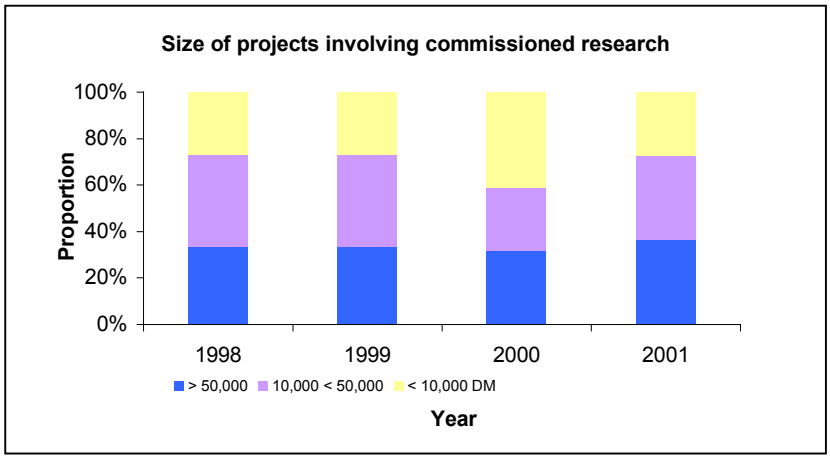
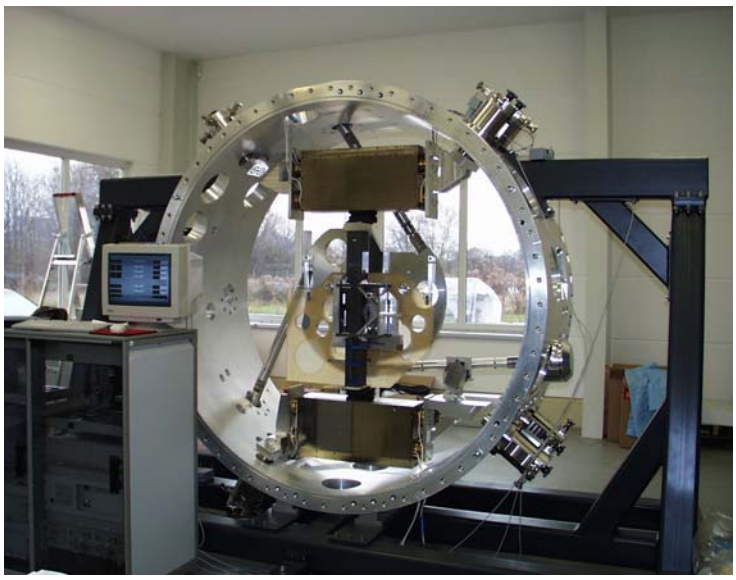


Fig. 5: Size of projects involving commissioned research

Mechatronics



In the Mechatronics Department, precision drive systems are designed, analysed and tested for the most varied fields of application. The work involves not only design and construction but also optimisation.
This last is achieved by modelling and simulation of the heterogeneous systems, which are in some cases extremely complex. The modelling permits accurate and dependable predictions of the systems' behaviour, for example in respect of mechanical deformation, dynamics, and magnetic or thermal behaviour, so that the number of design cycles is reduced to a minimum. The tools used for the purpose include Ansys, Maxwell and Matlab/Simulink. Design and construction is supported by Mechanical-Desktop or Pro/Engineer.
The subjects addressed by the Mechatronics Department -

- direct drive systems
- drives for use in UHV
- devices and instruments for analysis, and
- complex mechatronic systems

do, of course, overlap even within the Department of Mechatronics, while at the same time having close links with the systems design, circuit engineering and measurement fields.
The approach in project work is particularly to take a holistic view of the system and its optimisation. Close interdisciplinary co-operation between experts combined into project teams and staff from the commissioning company is always the pattern.
The drives that have been designed at IMMS have the following characteristics, to take some examples:

- high accuracy and excellent dynamics even in multi-track movement (in the case of multi-axial direct drives)
- the employment of a variety of physical bases to the movement (e.g. electrodynamic, electromagnetic or piezo-electric).
- control by means of systems with innovative strategies

The Mechatronics Department designs innovative drives as tailor-made solutions or applications and adapts them with suitable sensors and control systems before integrating them into plant and equipment. The Department also commands considerable knowledge with which to design plant by combining conventional drive, sensor and control components.
Measurement and control systems are available in plenty to help us assess and optimise the drive properties and to carry out rapid prototyping when designing the best regulatory software.
Currently, we are in process of developing and investigating:

- magnetic bearings for shafts (p. 10)
- drives for HV and UHV Applications (p.14)
- plant and components for MEMS-Fab fabrication of micro-electrical mechanical systems (p. 12)
- sensor and control systems components for planar hybrid stepping motors (p. 8)
- 5-axis positioning systems for high-precision polishing of fine optical components (p. 7)
- systems for the adaptive identification of load and centre of gravity for precision drives (p. 16)
- drive system for a 3-D precision gauge (p. 13)
- planar electrodynamic direct drive systems
- micro-tribology systems
- design of digital regulating systems with multiple axes.

Tasks we envisage for the future are:

- design and implementation of track control systems for multiple-axis drives
- drives for stepper systems and lithography systems
- optical surface measurement technology.
- positioning systems for the nanometre range and wide fields of movement.

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The Design, Construction and Testing of a Positioning System with 5 Axes

Objective

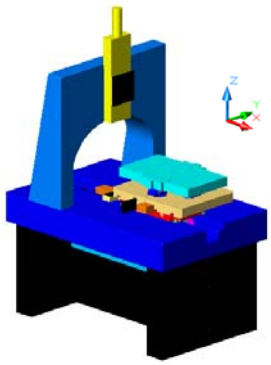
In recent years, the Department for Mechatronics has acquired considerable knowledge on the subject of drive systems with magnetic bearings and air guides, particularly in respect of positioning and drive systems for use in laser cutting and other work. At the same time as the mechanics were mastered, there was spin-off in respect of control systems construction. The controls have so far related to dual axis drives. However, positioning systems for 5 axes, and the relevant controls, are necessary when it comes to polishing optical components - which raises a new challenge. The need is for travel in the *x, y* and *z* directions and for positioning accuracy of 10µm or even 2µm, while the distances travelled are no more than 400mm. There is also a need to provide for tilting round the *x* and *y* axes by 5°, with accuracy of this angle down to ≈ 4". The tools being moved weigh ≤ 10 kg and they must keep on track with accuracy of ±10 µm. The positioning system for this purpose is being developed in a joint project with the Friedrich Schiller University in Jena. The project includes the construction right through to the testing.

Progress and status of research

Within the project, the research is focussed on:

- working out the principles for the programming of the individual movements of the equipment, and selecting the relevant ones
- designing the regulator and incorporating it into hardware
- selecting the sensor principle, designing and constructing sensors plus related electronics
- 3D designing and constructing a prototype

To permit virtual exclusion of mechanical interference (vibration in particular), the choice fell on a solid granite table. A one-piece gantry, also in granite, was set on this table to secure the z axis. A conventional module with high-resolution was used for this (z) axis. A linear direct drive powered by electricity sets the x and y platens in motion along their respective axes. These platens travel individually on four air glides over the granite base. The x platen glides along its axis with motion given by smoothly functioning magnetic bridges and air bearings, on a guide surface of extremely high accuracy, which is embedded in the granite base. The air glide for the y platen is along a high-precision guide in the form of a beam borne by the x platen. An optical linear measuring system is used in each case to register distance travelled. The tilting plate is carried on the y platen by means of a high-precision universal joint. Tilting is triggered by four "Voice-Coil" direct drives positioned symmetrically on the underside of the tilting plate at its edges. There are high-resolution, modified linear gauges to measure the change in angle on either side of universal joint. The dimensions of the positioning system are 1,200mm x 800mm x 1,700mm, and its weight is approx. 1000kg. An industrial computer workstation is used for the movement control. The whole construction is contained in a 12 HE cabinet (HE are units of height).



Outlook

The drive as it is designed is well matched to the demanding specifications, on account of the impressive stiffness of the air bearings and granite base. The direct drive components selected are a further great advantage. The desirable features achieved by the air bearings and direct drives are the non-contact mechanism and resulting durability; the almost infinitely reproducible accuracy; the freedom from stick and slip; and the regularity of the movement trajectories.

The software accompanying the system is being extended so that programs for the movement written in G-code can be read. The co-ordinates tapped in for the trajectories are converted into the relevant co-ordinates for the data processing system. This conversion involves adding trajectory points in such a way that the movements on the various axes will take place simultaneously. A selection of interfaces is installed to accommodate the customer's own manufacturing system. The user interface offers a visualisation of the planar curve in the x and y plane and the current position of the drive axes. It also permits limiting values to be tapped in. If the system detects any problems, such as loss of compressed air or movements beyond the limiting values, the error handling software will toggle the manufacturing system into error mode and interrupt the manufacture. All the software for the control system has been created by in-house engineers.

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Non-linear control of step motors, including sensors for position measurment and algorithms for error recognition

Objective

Mechanical engineers all over the world are being required to achieve ever higher speeds and levels of accuracy. There is a trend towards the use of direct drives, which will avoid the problems of classic rotary spindle drives: the loose, friction, noise and elasticity. The fact that there is no gear box with direct drives reduces size and weight and improves the dynamics. In the attempt to exploit all the advantages of precision and speed offered by the design of direct drives, it is not enough simply to use them as a classic step motor with open control loop. The drive itself needs a system for position measurement and control. As part of a joint project funded by the TMWFK, the Thüringen Ministry for Science, Research and Cultural Matters, new-type, non-linear algorithms are being developed to control step motors. IAS, the Institute of Automation and Systems Engineering, has the task of designing the control systems, and IMMM, the Institute of Microsystems, Mechatronic and Mechanical Engineering, is contributing the dynamic model for the drives. For the positioning and track control, the achievable performance is actually a function of the features of the regulator and of the quality of the position signals registered. The development of a measuring system which can be integrated into the drives is being undertaken by IMMS (the Institut für Mikroelektronik- und Mechatronik-Systeme gGmbH Ilmenau) in the context of the joint project. The signals from the gauge must be able to serve as input values for extremely fine control systems. IMMS is concentrating on gauges for planar drives as there have been none of these on the market at a reasonable price with sufficient robustness and accuracy.

Progress and status of research

A number of basic physical principles where considered within the project to see if they are suitable for measuring sensors. The outcome was that the only feasible means of creating a "ruler" is to use the teeth on the stator. Any other solutions mean planar drives, in particular, will be limited in choice of installation position and thus unable to be used in many otherwise appropriate situations. The alternatives also proved to be more susceptible to dirt intrusion or other problems from the environment. In addition they were more expensive and much more difficult to run.
So it was with a variety of measurement systems using the stator teeth that the research continued. Optical, capacitive and magnetic principles were all looked at. The procedures based on these principles were judged on the following criteria:

- performance, especially in respect of resolution and accuracy
- robustness in the face of interference or ambient influences
- durability, maintenance requirements, cost.

in addition to the sheer technicalities of manufacture: the difficulty of assembly and / or integration into existing systems. The conclusion from all these investigations was that magnetic scanning of the stator teeth provided the best compromise in response to the various (and sometimes contradictory) criteria.
As the project proceeded, detailed studies were made to decide on the best shape and material for the scanning sensors. It was possible to accelerate the optimisation by taking electrical substitute models as a preliminary to the time-consuming FEM simulation. Using the substitute models, correct deductions about the relationship between the signals and the geometry and / or materials were made. Only with respect to the form of the signal sufficiently accurate prediction was not possible. The reason for this was that a substitute model did not permit absolutely accurate reproduction of the changes in magnetic resistance within the air gap while the sensor is moving. Here 3D FEM simulation, however time-consuming, was indispensable on account of its accuracy.
The optimisation goal was a signal amplitude as great as possible, with a signal as close to a sine wave as possible, so that signals could be easily read. In addition, the signals needed to be very robust in the face of interference and to offer considerable tolerance. The studies conducted into parameters revealed that both goals were not possible to score in one solution. With the project partners at LAT (L-A-T Linear Antriebs Technik Suhl AG) it was therefore agreed to develop and test two solutions. Experimental investigation of the new sensors showed that measurement error from a simple atan registration was lower than that of the initial solution suggested (see fig. 1).

Outlook

Future work is to concentrate on developing and algorithm to permit automatic error recognition, and correction of measured values so that the system is even more accurate. It will also be necessary to integrate the sensors into designs for non-linear regulation, with the aim of proving that these sensors are the means of achieving track-controlled planar step-motor drives of extreme precision.

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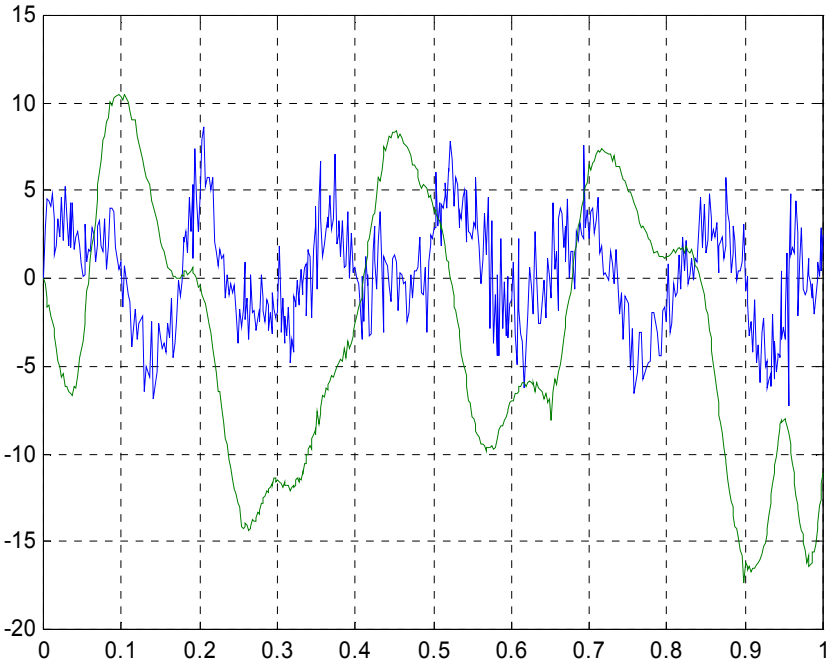

Fig. 1: Measuring error compared: initial solution (green) as against optimised solution (blue); a laser interferometer provided reference measurements

Design, construction and testing of magnetic bearings for high-speed laser rotary compressors, assuming state-of-the-art control systems

Objective

Magnetic bearings have come to be used in a wide range of applications in recent years because they require no maintenance and involve virtually no friction. These characteristics make them ideal for use in vacuum pumps and compressors, for instance. The higher speeds of revolution consequent on reduced friction permit a leap in the dimensioning of the pump capacity. Stoppages are avoided because of the low maintenance. This helps greatly to reduce general running costs, as compressors are often essential parts of such expensive industrial plant as high-performance lasers.

So that the individual details of the magnetic bearing within its system can be taken into account from the first, it is best to design the functions of the shaft and bearings as one whole. This method is effectively a re-design of the shaft and, as it involves expense, is not always applicable to conventional manufacturing situations. What frequently happens is that the shaft is re-designed but its functional components remain unchanged, and the conventional bearings are replaced by magnetic ones.

Currently IMMS is involved in a joint project with Becker GmbH & Co. with the aim of re-designing a high-speed laser rotary compressor. The work entails the development, construction and testing of magnetic bearings to match given specifications, such as a shaft weight of approx. 20 kg. The project began in September 2000 and is being funded by the Thüringer Ministerium für Wissenschaft, Forschung und Kunst (Thüringen Ministry of Science, Research and the Arts).

Progress and status of research

The foci for the project are

- Evaluation and selection of the principles of magnetic bearings most relevant to the intended industrial mass production and associated cost factor
- Simulation and design of the 2 radial bearings and the axial bearing
- Design of the regulation mechanism on the basis of simulating how it works; design of hardware to implement
- Selection of sensor principle, design and construction of sensors plus related electronics; design and construction of the triggering electronics in the regulating coils
- Re-design of the housing elements and the support for the magnetic bearing
- Construction and testing of laboratory samples and prototypes.

The magnetic bearing makes use of the force of reluctance generated between the iron ring and the air gap. How this principle is used in practice will vary: a distinction is made between radial magnetic bearings on the basis of the flow density in the iron ring. Operating across or along the shaft, they are hetero-polar or homo-polar respectively. They are also distinguished by the number of poles (3 or 4) and the type of pre-magnetisation (permanent magnet or coil-magnetised). In addition, if permanent magnets are involved, the axial bearing can be magnetically coupled into a compact unit with one of the radial bearings.

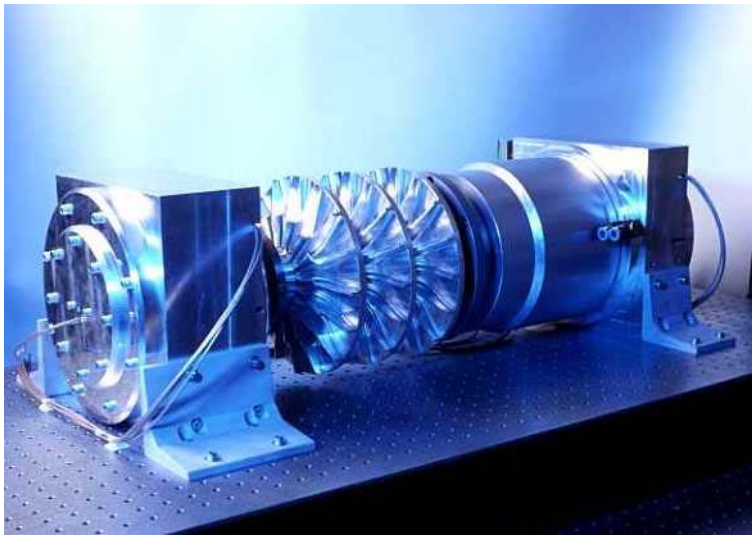

Fig.1: Experimental sample of the shaft with magnetic bearing

From the various bearing types, it is necessary to select the best bearing in respect of achievable strength, geometry, resistance to heat, difficulty of manufacture and manufacturing costs. The foundation for the selection process is a two-stage model. An FEM model to establish the fine detail is superimposed on the basic analytical model used for the rough dimensioning. The investigation included an analysis of a matrix devised for evaluation purposes, and led to the conclusion that the best radial bearing was hetero-polar with 4 poles. Although a bearing system based on permanent magnets offers great advantages from the point of view of volume taken up by the bearing, the increase in cost over a purely electromagnetic system is a contra-indication.

The shaft with its 6 degrees of freedom was seen as a coupled system when it came to designing the regulator. The various masses were concentrated for the modelling of the shaft. The model of the shaft was then validated by taking measurements on the shaft (a modal analysis) and using a FEM volume model in ANSYS. For the experimental sample, the implementation of the regulator used the rapid prototyping system "dSpace", and was realised in hardware that had been optimised in respect of functionality and cost. Eddy-current sensors generate the inputs to the regulator.
The compressor shaft, stator and housing components which were to receive the magnetic bearing were re-designed to improve this prototype. Revolution speeds of 15,000 rpm were achieved when the regulator filters had been optimised. These speeds represent the achievable maximum under normal atmospheric conditions in view of air friction.

Outlook

Future work will concentrate on sealing the prototype under vacuum so that the for the compressor shaft's nominal revolution speed of 30,000 rpm in a closed gas circulation system can be achieved. An attempt will also be made to substitute purely electromagnetic bearings, which have already been designed, for the permanent magnets at present used in the experimental sample.

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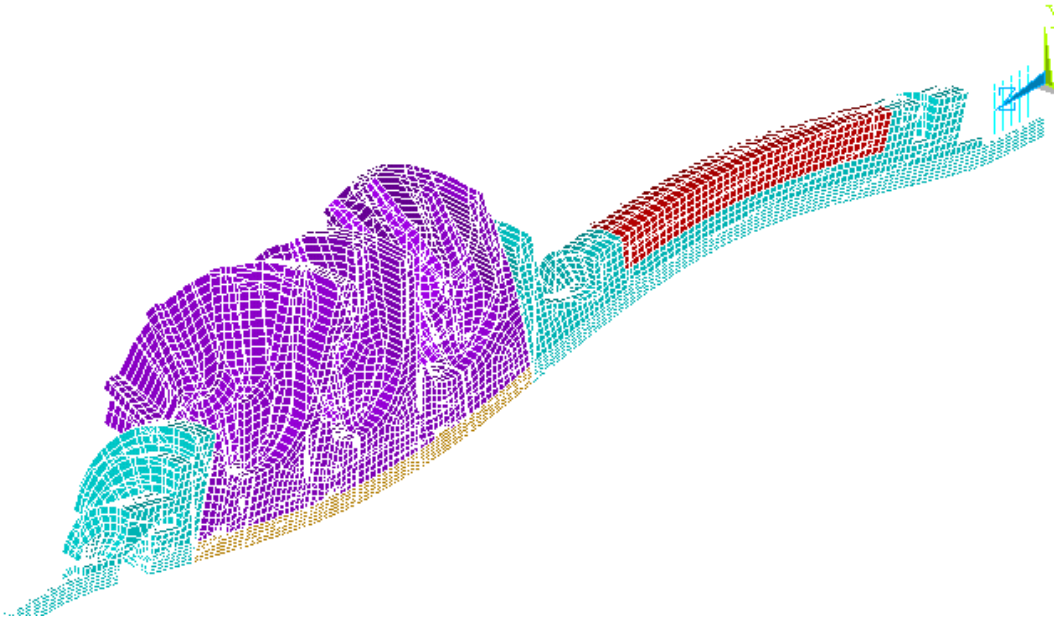

Fig. 2: FEM simulation of the second flexural wave of the compressor shaft

MEMS-Fab: Fabrication of Microelectromechanical Systems

Objective

Small and medium sized enterprises (SME's) the world over are looking more and more to manufacture, at more efficient and economical rates, products that come out of R & D. The comparatively small quantities - limited series, for instance - and the many different end-user problems requiring the SME's to provide a solution, mean that the process chains need to be flexible, which in turn means they should take the modular form, so that changing demands meet with rapid response. Individual steps in the process might be switched round, or additional testing procedures introduced. Small series manufacturing plant replaces expensive cleanrooms, for instance, with vacuum chambers or inert gas chambers. It offers flexible linkage of preparation, assembly and finishing processes which have already been tried and tested and which only have to be adjusted to the quantities expected or space available.

Progress of Research

The objective of the project is the development of a modular system, which will be independent of the external environment, to manufacture small and medium quantities of mechatronic products. The demonstration model being realised will make it possible to produce sensor and activator components by using photo-structurable types of glass (see fig. 1). All the manufacturing process steps are carried out by established technological methods and processes. The following points have so far been covered:

- Selection and adaptation of conventional, process-specific small series assembly equipment such as surface-finishing apparatus.
- Further development of conventional containers, locks and pumps.
- Adaptation of the analytical hardware and software to permit determination of workpiece/samples parameters without interruption to the process
- Achievement of flexible linkage by development of universal coupling units.
- Idea, design and construction for universal transfer and handling systems
- Idea, design, and construction for process-control systems

IMMS' part in the project is:

- the overall design for the demonstration plant
- conception, development, construction and testing of experimental setups of the necessary drives and the handling systems,
- the grab equipment and the magazine systems
- Conception of the interconnection of the process chambers, of the transfer systems, necessary for the goods to pass from one process chamber to the next, and the drives for them.

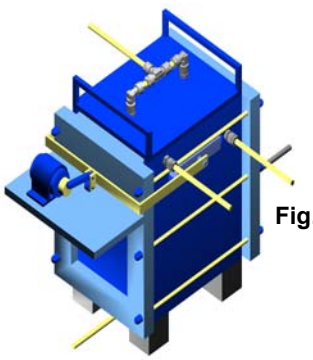

Fig. 3: experimental setup of the tempering module (source: TU Ilmenau)

Status of Research

Three modules have so far been created:

- the wafer illumination module (TETRA GmbH, Ilmenau, IMMM, and IMMS, fig. 2
- the etching module (ILMVAC GmbH, Ilmenau TU's Department of Glass and Ceramics Technology and Department of Construction Technology, and IMMS), fig. 3
- the tempering module (LMS GmbH and Ilmenau TU's Department of Glass and Ceramics Technology).

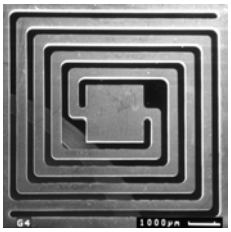

Fig. 1: Example of a sensor component, made of photo-structurable glass (source:TU Ilmenau)

Fig. 2: experimental setup of wafer illumination module (source: TU Ilmenau)

Outlook

A follow-up project is planned to develop further modules and their linkage, so that automated manufacturing of sensor components from photo-structurable glass can be carried out from start to finish.

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Development of a Measuring and Drive System for a High-Precision 3D Gauge

Objective

It can be predicted for both general manufacture and the fields of micro-mechanics and microsystems that in future the registering of fine details of shape in ever greater complexity down to the nanometre range of resolution will be indispensable. There are, however, to date, no accurate high-resolution gauges available to carry out 3D measurement of bodies with linear dimensions between 0.1 mm and 1 dm. The current project is thus devoted to establishing the principles for such a high-precision 3D gauge. Certain designs for planar drives are being investigated which will accept simultaneous incorporation of laser measurement by interferometer into the overall design. Basic principles for the spatial measurement of bodies contained in a measured space of (100x100x10) mm^3 are thus being decided on. A supplementary laser interferometer to probe the samples in the z direction effectively provides the required 3D precision gauge. Drive solutions involving planar direct drives with air bearings are being investigated by IMMS in the context of a DFG (Deutsche Forschungsgemeinschaft) project. Two other partners in the project are the Prozessmess- and Sensortechnik FG (Research Group) and the Antriebstechnik FG, at the Technische Universität Ilmenau - studying process and sensor measurement, and drive technology respectively. They are tackling the layouts required for position sensing with a high degree of accuracy and for the use of magnetism to guide the objects through the space where the measurements take place.

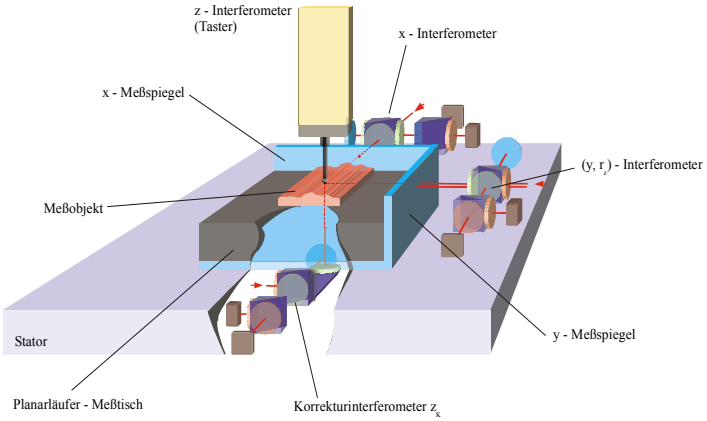

Fig. 1: Representation of the overall design for the precision gauge

Progress and status of research

The aim of the project at IMMS is to create a multi-axial direct drive with a stick-slip free glide, for a 3D precision gauge to measure (100× 100× 10) mm^3.
Such a concept requires the engineers to generate travel and movement (and the necessary forces) in a total of three linear axes (x, y, and z) and round one rotary axis (r_z). In the first (two-year) stage of the project, the z element is being registered exclusively by readings from a sensor mounted on a gantry. This sensor also registers if the stage itself changes in height on the z axis. On account of their high attainable speeds and fine control potential, electrodynamic motors are the preferred choice to generate the forces moving the object to be measured through all the various individual coordinates. Special attention is being given to the problems of form and layout of the magnets and coils to generate the forces and the motion. This stage of searching for structures and forms has the goal of the best possible integration of all the drive axes into a compact system of motors with a rigid structure.
It is also intended to design and test a stick-slip free glide, based on optimised air bearings, for all co-ordinates, with minimal departure from the set course.
As the drive system - i.e. the motors and glides - must also make it possible to integrate the interferometer as neatly as can be managed, so that the measurements achieve high precision, the work on designing the gauge is being carried out in close collaboration with the TU's Dept. of Process and Sensor Measurement.

Outlook

The main focus of the work at IMMS is currently on the total gauge design, with attention to adapting the measuring systems. Thereafter it is intended to construct the motor, assemble it, set it up and subject it to lab tests. The glide for the stage, or forcer element, will require particular attention. To achieve the freedom from stick and slip which is essential to precise positioning, the intention is to integrate aerostatic glide elements into the stage.
Schemes must also be worked on to enable tracking error to be recognised, calibrated and, where necessary, compensated for.

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Regulated precision drives for difficult operating conditions

Progress of Research

The focus of the joint project was the development of mechatronic precision drives which, at the same time as achieving high accuracy (and/or reproducibility), could be used under severe operating conditions, such as ultra-high vacuum (UHV). It was possible to create experimental setups and demonstration models which proved that modern materials and combinations of materials make the use of precision drives possible under harsh operating conditions. The range of positioning accuracy attempted is that below 10nm or a few hundredths of a second of an arc.
The following tasks were tackled:

- the development and construction of measurement and analysis systems, such as tribometers, specific to the materials being tested, and the testing itself
- development, construction and testing of the elements of the rotary and/or horizontal drives generating movement; also of further components
- the development, construction and testing of sensor, measurement and control systems which have been specifically designed for the application
- development, construction and testing of model mechatronic drives for problematic operating conditions such as UHV.

The materials, both separately and combined as layers, were thoroughly investigated in respect of desorption behaviour and tribological properties under predefined conditions of use, for instance. The tribological investigations provided considerable information for future reference if the materials come to be used in glide or roller bearings or tracks. Within the project, the tribological properties of a variety of materials and combinations of materials were studied to establish friction and wear data, particularly desorption behaviour, and to obtain specific answers where there was a question of their suitability for particular environments. To take the tribological investigation into the field of normal atmospheric pressure and of high and ultra-high vacuums, a variety of pin-on-disk or oscillating micro-tribometers and other testing equipment was produced. With the equipment, investigations can be carried out on alternative combinations such as ball-on-surface and surface-on-surface.

Status of Research

The fact that the oscillating micro-tribometer works on five axes under normal atmospheric conditions means that the samples being tested can be lined up parallel to one another. It is thus possible to investigate the tribological properties of two flat samples at once.
For the investigations under vacuum, an oscillating vacuum friction tester has been developed (see fig. 1).
Using a seven-axis universal tester, pairs of samples can be arranged parallel to one another (with three lifting axes), brought into contact (with one lifting axes) and moved round in opposite directions to each other (with one revolving axis). It is also possible to move the upper sample, which is fixed to the sensor head, through 90° (with one swinging axis). The possibility of a hemispherical exploration of the lower sample is thus opened up. The normal force to be set between the two samples at a defined level is produced by a piezoelectric drive (on one axis). The universal tester has optional extra drive and measurement systems such as an x-y table. Adhesion, indentation, and hardness measurements are possible in addition to tribological (oscillating and pin-on-disk) investigation of materials.
Tribological investigations in the micrometer range following the pin-on-disk principle can be carried out with both the tribometers featured in figures 2 and 3. The microtribometer in figure 2 is suitable for investigations under normal atmospheric pressure. The microtribometer for investigating

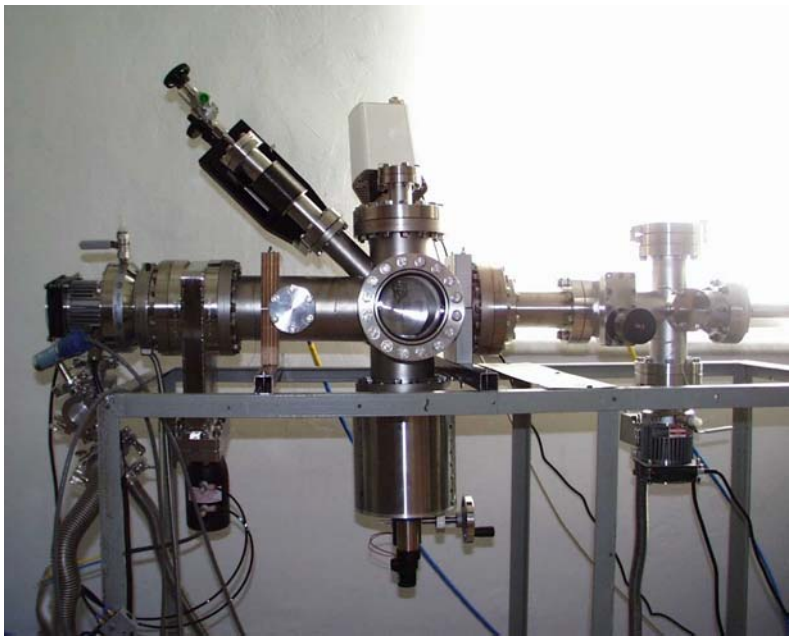

Fig. 1: Vacuum oscillation tribometer for pin/surface paired samples

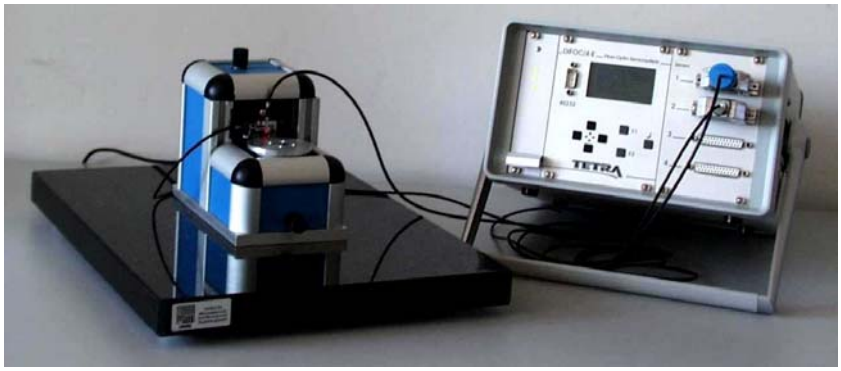

Fig. 2: Pin-on-disk microtribometer for normal atmospheric pressure

surfaces under UHV, which is shown in fig. 3, is fitted with the same drive, a piezoceramic motor with lamellae specially developed for this application by the PI Ceramic company. In both testers, the same principle for recording measurement data is used. They thus permit comparative investigations of samples under either atmospheric or UHV conditions.

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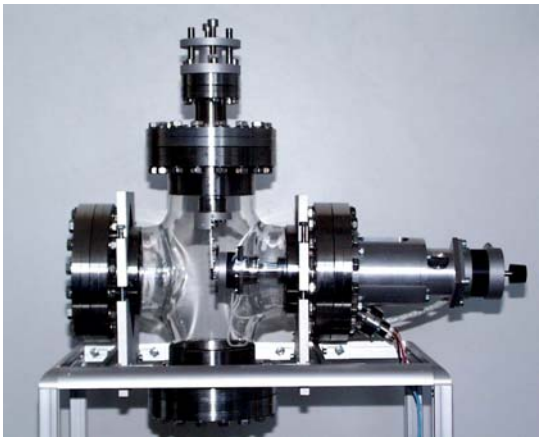

Fig. 3: Pin-on-disk microtribometer for UHV

Improving the quality of planar drive controls by identifying load features

Objective

The industrial demand for drives for positioning systems coping with distances from small (a few dm) to tiny (a few cm) is on the increase, especially in the high-tech field, and mainly in the linear and planar dimensions.
The parameters which are crucial, because they set a limit on the efficiency of the drive in operation, are the speed attainable and the accuracy of positioning or track-following. A precision drive system which IMMS and the TU Ilmenau jointly developed has long since passed the prototype stage and is now well-trusted in industrial use.
Its drive system is flexible and can be adapted to a customer's particular track or positioning requirements with no difficulty. When this is done, the dynamic parameters for the forcer are modified by the change in weight of the various carrier platforms or the stock itself, because the centre of gravity is shifted.
Each instance of actual use with a load will thus affect what are the best parameters to set in the control system, which was designed on the basis of a single model. A dissertation for the German "Diplom" (equivalent to M.Sc.) is being devoted to the investigation of mechanisms and algorithms, the former for adaptation and the latter for identification, of relevance to the use of this actual precision drive.

Progress of Research

The actual control settings with which the operator responds to his or her observation are first to be recorded for a plant. Preliminary investigation has already shown that the control system structure thus selected and recorded is astoundingly robust in respect of the parameters for this class of plants and their (limited) variations. There is still scope for adjusting the parameters of the controls and of the observer to the relevant data, to allow the high potential of the control system to be fully exploited.
The first step has been to derive model equations for parameters of relevance to the design parameters aspired to. The aim was to express the model in a sufficiently accurate description, using the simplest possible mathematics.
When a comparative test of a variety of identification algorithms was run, it was found that a parameter estimation algorithm based on R. Kulhavy's **restricted exponential forgetting (RXF)** method was best, especially for its performance in the closed adaptive circuit. The method is robust and reproducible.

It is now intended to make the adaptive mechanism respond independently to plant parameters which may be in part unfamiliar. This tuning will in effect involve a suitable combination of identification and design. As the intention was always to use an ADSP 21060 board as

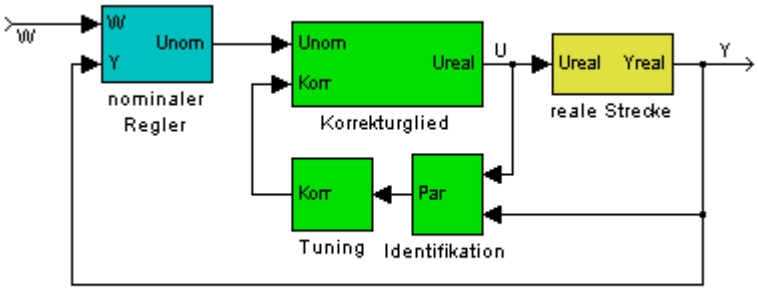

Fig. 1: configuration of the adaptiv system

the hardware, design methods requiring huge capacity were ruled out from the first. The pattern shown in fig 1 offered flexibility of both interpretation and realisation.
The most promising approach was applied on a rapid prototyping system, having been selected according to principles derived by computing simulated runs with MATLAB/Simulink. The ACE-Kit 1103, produced by dSpace GmbH, was employed to power a demonstration model planar drives via the relevant terminals with correct input.

Status of Research

When successful test runs had taken place, a reference contour was selected within which it was possible to assess and compare control sstems with and without the adaptive algorithm. An array of 10 x 10 circles composed the reference contour. Each of these circles had a radius of 84 µm. Different loads were fixed to the forcer in the appropriate manner but all other variables were kept constant. The variation from the reference contour of the actual path travelled was investigated.
Three criteria were evaluated in respect of each circle in the array:

- the average deviation (MITAB) from the reference radius during the following of the circle
- the maximum deviation (MAXAB) from the reference radius during the following of the circle
- the maximum variation in the radius of the "circular" track (MAXRS)

As is shown in fig. 2, where the quality is shown in without (blue) and with (red) the adaptive additions respectively, the adaptation brings the quality into almost total congruity

with the nominal quality of the system as designed, whatever the load situation.

Outlook

There are now plans to transfer onto the hardware (a MCX-DSP board from PMDI) the adaptation researched, and to integrate it into the existing softwareproject. It was certainly advantageous to take account of the limited hardware resources in the intended application from the very start of the decision-making for the research.
Now it will be a question of formulating algorithms for monitoring and certainty, which will guarantee certain marginal conditions, known as identifiability features, with the effect that adaptation takes place only when the changes in the dynamic parameters have been incontrovertibly recognised.
Another development will be proving that principles of the adaptive programme approach will work for other drives.

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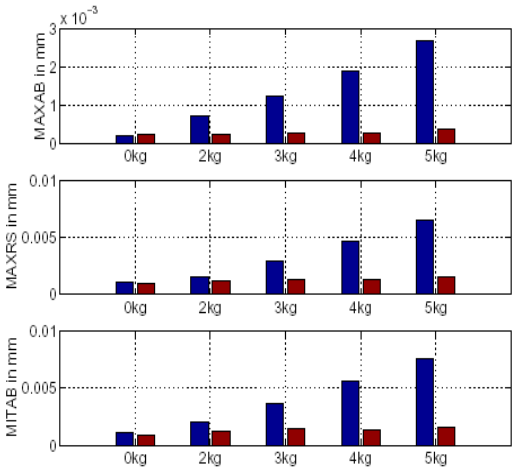
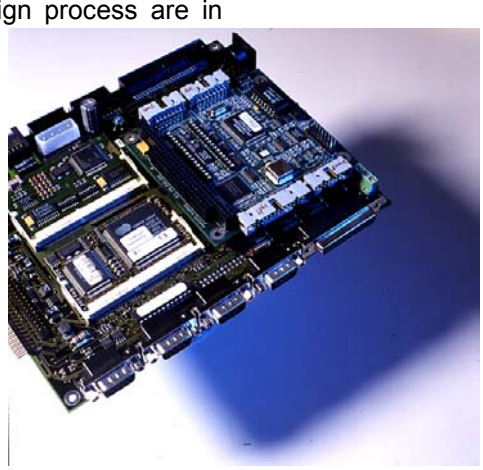


Fig. 2: Quality plotted against load

System Design

The System Design Department is researching the design and realisation of complex embedded electronic systems. The use of start-to-finish development processes which are based on a design flow specific to the application and the architecture is indispensable. In this context, a highly complicated electronic system is first modelled and then a simulation at the abstract level gives a behavioural description, so that the system can than be gradually synthesised, implemented and integrated. The abstract modelling takes place with the aid of such tools and methods as Statemate, Matlab/Simulink, HDL and System–C. The outcomes of the design process are in the form of hardware system solutions such as ASICs (Application-Specific Integrated Circuits), FPGAs (Field Programmable Gate-Arrays), classic PCB Designs Printed Circuit Board), IPs (Intelligent Properties) and SoC (System-on-Chip). On the software side, they may be branded software products and applications for embedded DSPs (such as SHARC and TI) and micro-controllers (such as x86, ARM, MIPS, NEC and PPC). The Department is engaged in interdisciplinary work on three subject areas.



One is ***Digital Signal Processing and Industrial Electronics***. Here a project on linear and angle measuring systems has been brought to a successful conclusion. The interpolating circuit which was developed was produced as a sample, tested and handed over for trials in actual use to the industrial partners in the project. The early months of 2002 will see the conclusion of another project on a similar theme, a high resolution optical illumination gauge with absolute encoding. In this subject area our main focus was on research into image processing. A highly complex demonstration circuit board was developed at IMMS, which could be used to solve complicated problems in industrial image processing. What is new in this work is that the image processing has been divided up into the hardware and the software section, and that an innovative modelling method based on System-C is being used. For the first time, this method permits fulfillable specifications to be generated.

In the second subject area, ***Buses and Networked Systems***, the work on the IEEE1394 firmware library was successfully completed. Our industrial partner was EMSYS GmbH Ilmenau and we produced a highly portable library of firmware routines which can be used on a high number of IEEE 1394 hardware configurations. In addition, a start was made on the development of a bus converter for serial buses, based on an ARM controller. The board developed as a reference is operated with embedded Linux (see page 21). The intention is to use it in communications between a variety of serial buses and field buses in automation settings. At present, work is continuing on the implementation of the peripheral driver, using IEEE 1394, S-ATA and CAN. The porting of the Linux kernel from 2.0.38 to 2.4.10 for the NET+40 processor which was used enabled IMMS to come into possession of know-how on embedding Linux, itself helping us to acquire a further project. This concerns the design of a software platform based on Linux for set-top boxes and digital television.

The researchers on ***Embedded Software and Automotive Systems*** were successful in the field of using embedded software for communications devices involving GPS and GSM. In cooperation with one of our long-term R and D partners, a new device was designed which employed the open-source operating system eCos (see page 23).

Together with the Mechatronics Department, work was done on real-time control systems under Linux/RT and one was developed for mechatronic drives using standard components (see page 19). The employment of such components when designing control systems reduces the cost of the hardware for control boxes by up to 60%. Initial contacts for future work with industry were made at the "SPS/IPC/Drives 2001" trade fair in Nuremberg.

UML and formal specification and verification are another area of research, in which further developments have been made by university students on placement. These studies will be continued in a project in respect of which IMMS has now applied for funding.

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Using Real Time Linux to control mechatronic drive systems

Objective

To fulfil the timing requirements so critical for mechatronic drive systems, it is usual to employ digital signal processors (DSPs). The commonest solution at present is to use a standard personal computer (PC) containing a DSP card, which is responsible for reading the signals from the movement sensors and for guiding the activators.
Such a solution tends, however, to produce high hardware costs because a suitable DSP

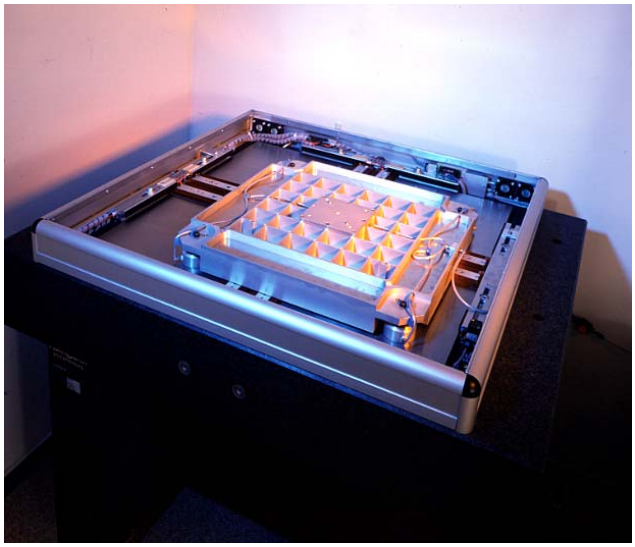

Fig. 1: mechatronic drive systems (for planar drive)

board is required in addition to the controlling PC. It is possible to reduce these costs by adopting a single-board computer with a standard operating system. To do so is well worthwhile when producing in large numbers. It is to be noted that the operating system used must be provided with a very finely determined time action in order for it to measure up to the timing requirements for these drives.
The hardware to regulate mechatronic systems is very reasonably priced if one uses an embedded PC with Linux as the operating system. The advantages are:

- operating system free of charge
- operating system works in real time - this is sine qua non for the control system
- high capacity hardware, which can "grow" as necessary
- all the functions of a normal PC, such as a variety of interfaces, TCP/IP, a screen, a keyboard and so on, available, without further costs, should they be required.

The adoption of a real-time operating system that will run on an embedded computer has drastically reduced the hardware costs for the control system. The specific hardware is an x86-based PC together with two converter cards (analogue-to-digital and digital-to-analogue). All the hardware components are standard systems. On the software side, the preference is for Linux, the freely available operating system, together with RTAI (Real Time Application Interface) as real time extension. The Linux/RTAI combination has no licence charges, permits latent interruption periods of mere micro-seconds, and is distinguished by its stability, scalability and ease of access to the source code. The present work has been the design of a module, both extendable and scalable, to regulate and control complex mechatronic systems.

Progress of Research

Over recent years, the Institute for Microelectronic and Mechatronic Systems (IMMS) in Ilmenau has developed considerable know-how on applications using PCs and Linux. The choice fell on Linux as an open source operating system with the RTAI extension for real time operation; the reason for this was the experience already accrued at IMMS and the need for a real-time system.
The project involved the following tasks:

- research into types of hardware, selection and testing
- searching for reasonably priced AD/DA modules, or modules offering interfaces between PWM (pulse width modulation) and encoder, where possible with Linux drivers
- testing of the AD/DA modules' suitability for the required type of regulation
- investigations into the processor performance necessary, using a sample controller
- purchase of selected modules and trials with the actual system
- integration into the real-time operating system
- regulation and control implemented as an RTAI application
- mechatronic control algorithms implemented as a real-time application
- realisation of a demonstration system.

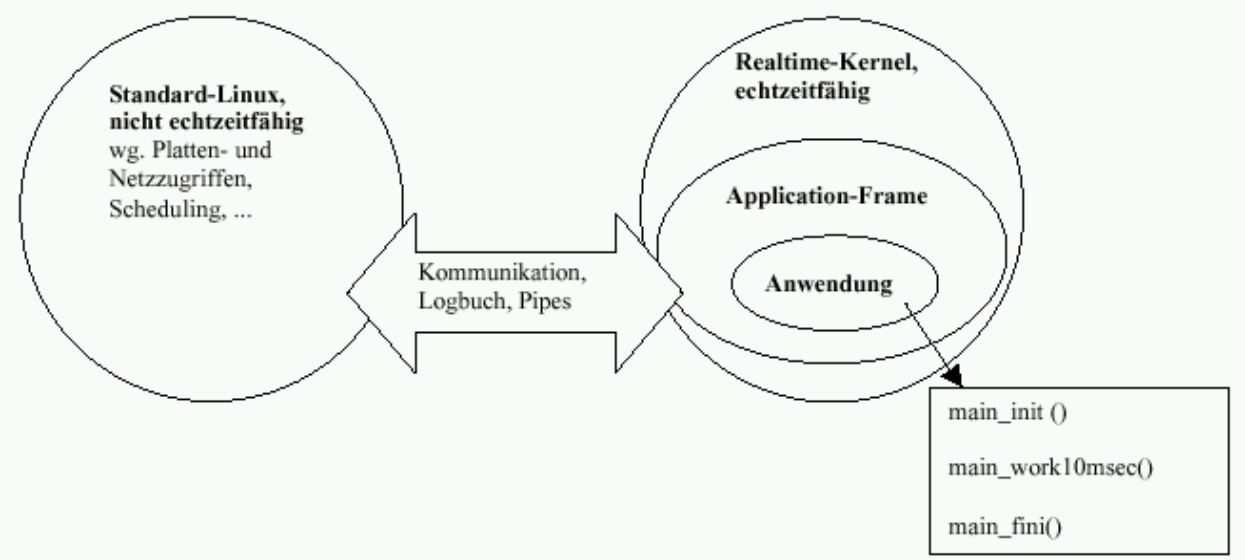

Fig. 2: Real-time operating system (relationship between standard and real-time Linux kernel)

Status of Research

A functioning control system, in the form of an RTAI Linux application, has been developed for a planar drive.
To achieve control of the regulation module (see fig. 3), a program was developed on the KDE graphic interface, communicating with the real-time regulating algorithm (the RTAI Linux task) via shared memory and first-in, first-out functions, (see fig. 2: Communication).
Currently, the frequency of regulation is 2 kHz, which permits the machinery to operate at 20 mm/s. Contained in the regulation module are the regulating algorithm and the controls for the two conversion cards (analogue-digital, digital-analogue), as required to drive the planar drive mechanism.

Outlook

Work is at present proceeding towards even shorter frequencies of regulation by optimising the software. The target is 10 kHz. For this purpose, the graphic interface is being transferred to a different computer. The module and the program controlling it will be linked for operation by means of a client and server system. This will produce economies in the computing time necessary and assist in raising the frequency of regulation. The entire regulatory system can be miniaturised if a PC with standard components is embedded in it.

The development of a design flow from the Matlab/Simulink model to the (RTAI) Linux control system as a standard process is a challenge it would be useful to meet in the long term.

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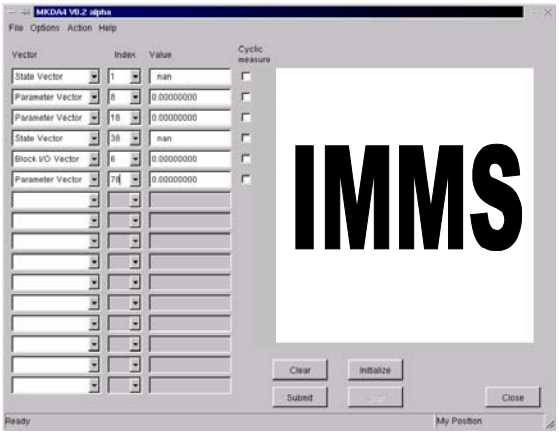

Fig. 3: The KDE interface of the program controlling the module

Embedded Linux

Objective

Now that Linux has been accepted on such a wide front as a freely available operating system, new fields of application are constantly being found. It is proving extremely flexible and useful. However, it has not yet come to very extensive use in the field of embedded systems, though it actually has great potential. Using Linux offers the following advantages:

- the free availability means that one is not dependent on a single manufacturer
- there is no licensing charge
- open-source projects which have already been created can be used
- considerable support is available from the community of Linux developers

IMMS has taken it upon itself to participate actively in spreading the use of Linux. The System Design Department is laying considerable importance on the operating system for the embedded market. Current work covers a wide spectrum, from hardware development to kernel portability and from developing applications and drivers to making use of real-time Linux.

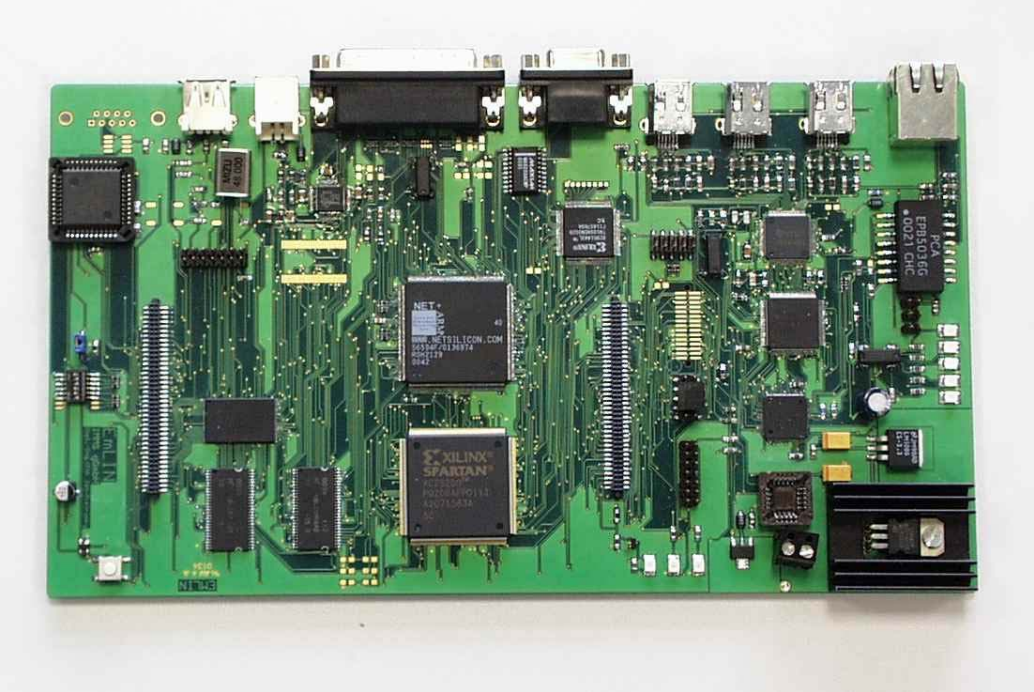

Fig. 1: The 250 x 130mm reference board

EmLIN has been developed as a means of conveying this know-how to our customers. The name EmLIN refers to a development board, based on a Net +ARM processor, for embedded Linux. It offers various interfaces which are used in industrial or personal computers. EmLIN was developed on a modular pattern, with the effect that the customer can compose his own system as desired from the components available. It is up to the customer whether to use EmLIN as a control system computer, as a universal bus converter for the transfer of a range of protocols, or simply as a Linux development circuit board.

Progress of Research

At the core of EmLIN there is a Net +ARM40 processor made by the NETsilicon company. The following components are necessary to ensure basic functioning:

- Net +ARM40 processor
- SDRAM and Flash
- an electricity supply
- Ethernet or RS232 as communication method

Equipped with these components, the board is fully functional. In addition, further interfaces of various different kinds are planned. The table below shows the full range of interfaces already available. There is also a freely programmable XILINX FPGA (field-programmable gate-array) available. This circuit permits additional hardware to be used, in which case a serial ATA protocol is programmed. Serial ATA is a new standard for connecting hard drives to a PC. It permits faster data transfer than did the conventional parallel ATA to date.

As the Net +ARM processor has no memory management unit (MMU) of its own, Linux for

Bus	Used in	Example
Ethernet	Office communications	Networked PCs, Internet
IEEE1284	Office communications	Printers
IEEE1394	Multimedia, PCs	Digital video processing
CAN	Automotive systems	Networked vehicle systems
USB	Multimedia, PC	Printers, scanners, keyboards
RS232	PCs, measurement	Sensors, gauges
Serial ATA	PCs	Hard drives

Fig. 2: Overview of busses currently in use

processors with no MMU is brought in as the software to solve the problem. The NETsilicon company supplied the development package, Net+Lx. It contains a cross compiler and a ucLinux with a 2.0.38 kernel. As the driver is available anyway, an up-to-date version of the 2.4 Linux kernel is used. The important thing here is that plenty of drivers already exist, and so it has not been not necessary to compose as many new ones. In the majority of cases, all that is necessary is a few changes to the source code in order to match the software to the hardware.

Status of Research

Currently, a Linux version 2.4 imported by IMMS is running on the EmLIN board. Work is now being done to match a variety of drivers to this version of Linux. The work on the serial ATA protocol has already reached the trial stage. Time is still required for the development of the driver, as it is necessary to write this from scratch.
The circuit is being constantly adjusted to the specifications. This applies also to the modularisation of the board, mentioned below.

Outlook

The components of one board are later to be divided across two boards. The actual core of the computer (the processor, the memory, Ethernet and necessary peripherals) will go onto one platen. The individual interfaces, a memory extension unit using SDRAM, and the XILINX FPGA will be installed on a mainboard of their own. As the requirements of industry are usually for sensors and actuators to be supported by a computer, there are also plans for extension to include two PCI sockets. It will then be possible to use cards from any manufacturer to collect measurement readings, or similar cards for the output of values.

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eCos - an Open Source Operating System for the realisation of complex embedded electronic systems

Objective

It can be said that embedded systems are increasing in complexity and that the appropriate hardware is available in principle; this is relevant both to applications which run in a main loop and to applications which even require an operating system within their embedded systems. It would be ideal for suppliers of complicated systems if each change in hardware did not require a new operating system. Ideally, also, the tools necessary for the development of the application and the operating system itself would not cause any additional costs. On account of its marketability, an R and D project has been devoted to a search for an appropriate operating system and a satisfactory development environment. The system selected must prove to be suitable to a complex embedded electronic system which is composed of a hardware platform and a demonstration application together with the operating system itself. The industrial partner in the project specified the functions to be possessed by the overall system, and the components of the hardware platform.

Progress of Research

Linux was the first choice for investigation. However, if, as is the case, the systems are to be marketed in large numbers, the resource requirements are excessive. Also, many relevant applications require less potential than is offered by Linux as operating system. An alternative was therefore sought.
The embedded configurable operating system known as eCos was investigated and found to be suitable. As it is an open source facility, there is no charge for its use. At the same time, the know-how for an application based on eCos remains the developer's and does not have to be made public.
Pursuing the idea of open source materials, the development tools used were also freely available. The cross-development tools (compiler, assembler, linker, debugger, etc.) based on GNU were used for the porting and the development of the application.
As the R and D project progressed, a decision was made on which controller to use. Other hardware components did not require a final decision at this stage. So that the porting did not have to wait until the actual hardware platform was ready, an initial porting onto a platform which was to hand was carried out. By doing this, the developers were able to recognise and cure certain problems at this very early stage. They could also check the eventual porting process for practical use. The knowledge thus obtained contributed to the subsequent, trouble-free and rapid import of eCos onto the hardware platform which had been constructed in parallel to these early experiments. Importing eCos involved four basic steps:

- matching the memory layout to the new platform
- porting a monitoring program to run on the platform, to control download and debugging
- adaptation of the serial interfaces
- integration of other hardware components

It became quite clear in conclusion that the "long way round" of first using available hardware was entirely vindicated. It meant that problems were dealt with early and the import onto the actual hardware platform was speeded up considerably.

Status of Research

eCos allows complex applications to be created. The operating system, which was developed by Redhat for such purposes, offers developers flexibility for their own programming, ensures that all aspects of the system are kept in view, and in this way provides maximum monitoring of the system itself. Not only this, but eCos will cope with real-time specifications. The functions made available by the operating system are:

- a variety of drivers, including Ethernet, USB, Flash and serial interfaces
- TCP/IP with optional SNMP support
- ISO C and mathematical libraries
- EL/IX level 1 Posix compatibility layer
- µITRON 3.02 compatibility layer
- RedBoot bootstrap and debugging firmware
- a hardware abstraction layer (HAL) which is eminently portable
- a real-time kernel

One of eCos' outstanding features is its enormous configurability. It admits not only of simple command lines but also a graphic configuration tool. It is thus an operating system which can be matched to the most varied of hardware platforms and trimmed to meet the specifications of the application in hand. Unlike Linux, which is for multiple users and multiple tasking, eCos is an operating system for single users and multiple threading.
The application is linked to the operating system under eCos and only then loaded onto the hardware platform. For instance, a test application which included eCos and had 3 threads took up only approx. 64 kB.

The functions listed above are not available in every case for every hardware platform. However, having a functioning example to hand means that one's own particular solution is easier to implement.
The import of the eCos package onto the new hardware platform has now been completed. The platform is shown in fig. 1. RedBoot, a standard monitoring program from Redhat, is also ported for downloading and debugging purposes. By way of application, a demonstration model was developed on the basis of the newly developed hardware platform with its eCos import. It makes use of eCos multithreading among other functions. The model served to prove that the newly developed complex embedded system was fully functional.
Our industrial partner has now, as a result of the R and D project and the use of eCos, a universal, highly adaptable, stable and effective operating system for real-time electronic programs, which is extremely economical with resources.

Outlook

The next goal is to transfer the conclusions from the R and D project to the industrial partner and to initiate their staff into the use of eCos. eCos is no different from other operating systems, in that it requires the developer to have no specialised knowledge of its internal workings before ideas can be expressed as applications. There is even the potential to modify the operating system if this is necessary to the demands of an application, thanks to the virtues of the open source, where eCos is found. This and other features of eCos mean it will be possible for any user to respond to future market demands in a flexible way. The result is that the use of the open source operating system eCos is superior to commercially available operating systems, and of particular interest to the developers and distributors of complex embedded electronic software.

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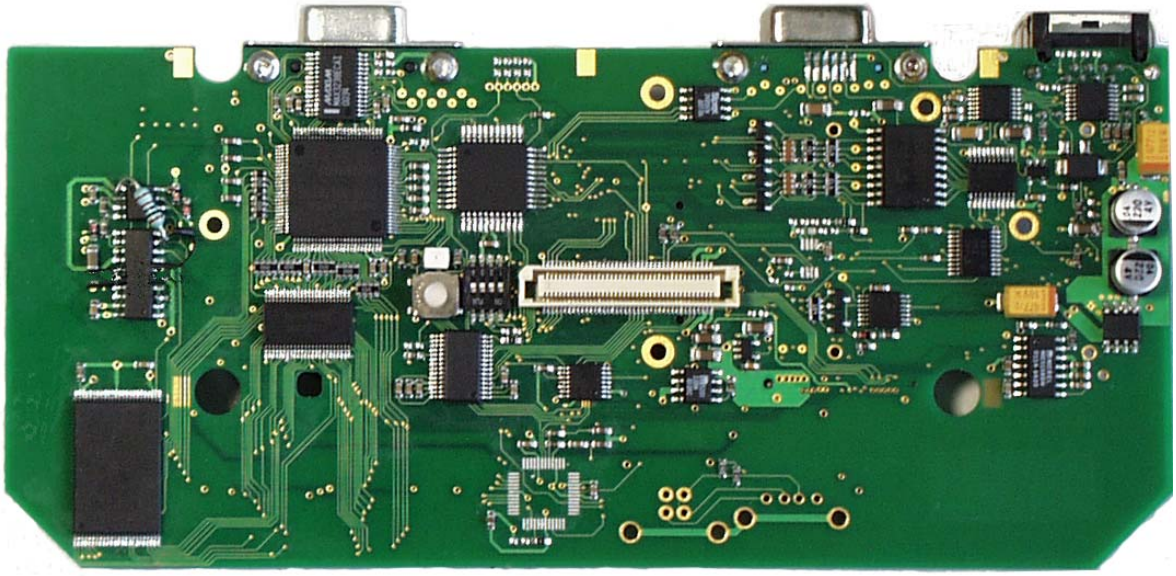

Fig. 1: Hardware platform

Circuit Technology and Microelectronics

One of the goals of IMMS is to improve the efficiency and performance of the design methods for analogue and mixed signal circuits, by researching into new circuit architectures and new EDA and design methods. The research is intended to improve the co-operation between the microelectronics and microsystems industry and ASIC design centres and companies who wish to perfect their products. The contribution which IMMS sees itself as making is to encourage innovation by working in interdisciplinary groups and competence clusters, such as OptoNet e. V. or Automobilzulieferer Thüringen e. V.
IMMS` work on mixed-signal circuit design has concentrated its competencies in the following fields:

- RF design
- ADC design and electronics linked to sensors
- optoelectronics
- DSP synthesis in mixed-signal ASICs, and synthesis based on control system
- modelling and simulation

The circuit engineering being tackled has the aim of making the research outcomes from European (MEDEA+) and national (BMBF) projects accessible to wide use, particularly by small businesses. The engineers bring their own skills and research experience to bear on the issue. At the same time, Thüringen's own enterprises in the microelectronics and microsystems industry, particularly in the Jena-Erfurt-Ilmenau "Technology Triangle", are being supported with research specific to their needs. They can thus develop their products with new, effective methods which guarantee-failure free results in a short time.
Outstanding outcomes of this policy in 2001 are:
A range of 433 and 868 MHz transmitter/receiver modules made available from industrial partners on the base of ***RF design*** research in the RF front end project (funded by BMBF) and the low power communications modules project (funded by TMWFK). Future research is planned for new SiGe and SOI technologies, with a frequency range of up to 6 GHz.
The ***analogue-digital converter group*** developed a 14-bit cyclical RSD ADC with behaviour descriptions methods. The development involved starting with the architecture and proceeding through simulation, optimisation, layout design and preparation of experimental samples. Progress was made at the same time in the design methodology for precision SC circuits. Initial work was carried out on Δ-Σ circuits and converters, together with the relevant filters.
The ***opto-electronics*** developers achieved a tripling of the switching speed for DVD reading units (TIA with > 40 MHz bandwidths) and circuits for read-write operation with a switchable dynamic range. An array of 512 photodiodes, including the analogue signal processing modules, was created to test high-resolution sensors with absolute coding. Research was started into circuits for low-cost optical buses.
Design methodology was developed for systems based on ***DSP***, so that a system can be first described in mathematical terms and then simulated, using MATLAB and SIMULINK. With this model as the starting point, resource requirements and attainable performance are now being investigated. The method permits subsequent implementation on a DSP emulator board, either in a FPGA or as an ASIC.
Modelling and Simulation had a period of rapid progress. The SOI group established the basis for modelling of SOI systems for X-FAB and also developed an SOI design kit for high-temperature digital and analogue circuit design. It was possible to produce successful first test circuits with the design kit and the CADENCE environment for Hall sensors, ADCs, SRAMs, drive control systems, etc., all working at temperatures up to 220 °C.
Further research is being carried out on new ESD test methods, ESD modelling and simulation.
Further work on new design methodology was carried out using EDA tools developed in MEDEA+ projects. From the ANASTASIA+ project the tools AnalogInsydes und AdvanceMS were evaluated, and from the VALSE project the Siemens verification software. The results will be capable of use in further internal research and training workshops.

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Analogue Correction Circuits for High Accuracy SC ADCs

Objective

In the ADC Department, 2001 saw the successful conclusion of the project with the German name "Entwicklung von A/D-Wandlern für die Anwendung in Digitalen Signal-Verarbeitungssystemen unter Berücksichtigung neuester Technologien, Techniken und Anforderungen", which is number B609-97049 supported by the Thüringen Ministry of Science, Research and the Arts and concerns the development of state-of-the-art analogue-digital converters. Two iterations in all were carried out for a cyclic RSD A/D converter using the CX06 cyclic technology from XFab in Erfurt. To provide a reference for our own set of measurements, the PTB (the federal german physical and technical institute) was commissioned to test the ADCs. The IMMS and PTB results agree very well. Two student projects, one for the "Diplom" thesis and one for a practical placement, were additionally devoted in 2001 to designing decimation filter for oversampled ADCs.

Progress and status of research

Once the first ADC had been successfully implemented, the research within the project in 2001 concentrated on analogue circuits for a correcting purposes, i.e. to improve the ADC resolution, of relevance for both cyclic and pipelined ADCs. This was to fulfil the constraints of using the ADC as a stand-alone minimal-area IP block (since a digital correction can be introduced in the digital section in any realisation of the design); and also as a circuit block to be used in conjunction with very sensitive switched capacitor (SC) signal-processing circuits, such as are required for capacitive sensors.

An algorithm has been developed, based on analysis of errors in SC circuits. The main work was on the offset and the finite gain of the operational amplifier (OpAmp). It was already possible at the stage of the first iteration for the ADC to suppress SC errors resulting from a capacitance mismatch, charge injection and cross-talk in MOS switches, by using appropriate circuit design, such as botom-plate sampling and a fully differential circuitry.

OpAmp errors in SC circuits

After the SC system has settled while in the integration phase, the finite gain and the offset of the OPAMP have the effect of creating a differential voltage at the inputs ($U_e=U_{out}/G$), which, in turn, means that the charge stored on the sample capacitance C_x derived from the previous sampling phase (see fig. 1a) does not get fully transferred to the integration capacitance C_y. Also, the voltage which appears at the output of the OpAmp is not the full voltage over the integration capacitance, but is reduced by U_e.

The charge balance equation for Cx to Cy transfer is as follows:

Given that $C_x=C_y$, the error amounts to $2 \cdot U_e$, which can be compensated for by means of an auxiliary charge ($Q = 2 \cdot U_e \cdot C_x$). The correction is based on error-sensing capacitances ($C_e \approx C_x$), which will, however, withdraw from the working capacitances a charge equal to the error which requires correcting. Thus, the error must be determined in an earlier "prediction phase", which "simulates" the actual subsequent calculation using dummy capacitances.

$$U_{out} = (U_{in} - U_e)\frac{C_x}{C_y} - U_e =$$

$$= U_{in}\frac{C_x}{C_y} - U_e\left(1 + C_x \Big/ C_y\right)$$

Correction Circuit

The second ADC design included an innovative correction process featuring charge addition. It is better than the principle so far recognised and used, that of voltage addition, and is particularly suited to realisation in fully differential circuit design. In this method, during the prediction phase, two measuring capacitances connected in parallel ($C_{e1}=C_{e2}$) between both OpAmp inputs are charged up to the full input differential voltage.

$$Q_e = U_{e1} \cdot (C_{e1} + C_{e2}) = 2 \cdot U_{e1} \cdot C_e.$$

During a correction phase, each of the C_e capacitances is re-connected between each input and the analogue ground (common mode potential). In the initial moments, voltage is doubled at the inputs ($2 \cdot U_{e1}$), an effect which is, however, counteracted and reduced to U_{e2} by the feedback, half the $2 \cdot U_{e1} \cdot C_e$ charge being transferred to the integration capacitance (C_y). If the conditions during prediction phase and sample phase are comparable ($U_{e1} \approx U_{e2}$) and if the design has ensured that $C_e = 2 \cdot C_x$, then the OpAmp error effect can be compensated for.
A disadvantage of the charge correction compared to voltage correction is the consumption of the charges at the C_e measuring capacitances during every correction phase. However, both C_es can be designed large enough to correct all errors of a multi-phase regime in the final phase.

Correction principle of ADC2

There are four SC-phase in our cyclic ADC, this number being determined by the SC block realising the mathematical function ($2 \cdot X_i \pm V_{ref}$). Two of these cycles are integration processes (based on charge transfers), which must be corrected. The error stored at C_e during the prediction phase is not used for correction until phase 4. The correction in phase 2 relies on a capacitance being re-used as integration capacitance during phase 2, after serving as a measuring capacitance during phase 1 where it was charged up to the negative equivalent of the error U_{e1}. A second SC block, sample-and-hold, forming a 3 phase circuit, is corrected by means of charge addition.

Physical Layout

Different layout styles were tested in both ADC iterations. Fig. 3 shows a typical, roughly circular arrangement of the blocks, which most closely suits the cyclic nature of the ADC operation, and thus avoids interference due to cross-talk. The crossing-free layout of sensitive nets was an important design criterion.

Results

The correction principle employed in the second ADC iteration (ADC2) proved functional as soon as the first dynamic and static measurements were taken. The characterisation of the ADC took place down to 16-bit-level resolution. Analogue correction improves the suppression of harmonic distortion, so that the original THD of -69.78 dB changes to -74.38 dB, thus positively affecting the overall ADC performance by shifting the SINAD (Noise & Distortion) from 65.77 dB to 66.80 dB. This corresponds to an effective resolution of 10.8 bit. It is therefore to be expected that a noise optimisation centred redesign would further improve the ADC. The integral non-linearity (INL) is found to meet the demands of the 12-bit level down to $\pm$ 0.5 LSB, as shown in Fig. 4. Static measurements not only show a lessening of non-linear distortion but also a reduction of the ADC's offset from initial 300-600 LSB units down to only 20 LSB units when using analogue correction.

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Objective

Control systems engineering products are often, of their very nature, manufactured in only small numbers. Their development represents a high proportion of their production costs. The proportion can be reduced by using mixed signal circuits with ADCs and DSPs. Being programmable, a single circuit can be modified for a variety of tasks and thus applied to a number of short runs. It has the further advantage of possessing the software to permit complex algorithms to be developed cheaply.
IMMS is developing the methodology for execution the signal processing tasks by means of combined ADCs, DSPs and other software.

Progress of Research

The year just past has seen further work on design methodology for these DSP-based systems, involving the development and configuration of design tools. The knowledge obtained was put to practical use in a demonstration design.

Estimation of Resource Costs

The choice of processor will have a definitive influence on the cost of any DSP-based system. The selection of the type of processor will be based on the main criterion of the technical suitability of the DSP, but also on other factors, such as the operators' state of knowledge and the availability of design tools.
Computing time and memory space are critical; to plan these aspects a program was produced which uses a model of the system to estimate the resources required (Fig. 1).
A model written in Simulink, a language for the description of systems, is analysed by the program and divided up into its algorithmic elements. The resources required on the planned processor are determined in respect of each of these. The estimation procedure is configurable. It is possible to add new processors in order to compare various processor architectures. The Calculation of the air-values and production of trial data were modelled in Simulink on a specification provided by Nord-Micro AG. The computation of the air-values was then programmed at IMMS in C for the ARC core. Differences between the ARC software and the Simulink model were analysed by simultaneous simulation of the two models. FhG IIS-A is implementing the system on an FPGA board and testing it.

Status of Research

hierarchical analysis of the use of resources then shows where they are being applied. Further work may then be carried out on critical areas in the system.

Simultaneous Simulation of System and Software

In the course of designing the system, one produces an executable specification in a high-level language such as Simulink or Saber. Refined models of the actual implementation are then verified in relation to the specification as the design proceeds. The use of other simulators for the implementation means that the data of the specification have to be converted, and the flexibility of the high-level language is thus lost.
However, the problem is solved if there is simultaneous simulation of the specification and the implementation (fig. 2).
The high-level language of the specification makes it possible to produce convenient test data. The simulator for the implementation permits precise simulation of the system designed.
At IMMS the high-level Simulink language has been harnessed to a variety of software simulators for DSP cores (ARC) and micro-controllers (MLX16). Because the simulation of the system model runs in parallel to that of the processor model, the two can be compared. The effect of differences between them, errors in rounding up or down, for instance, can thus be directly simulated.

An Air Data System as Demonstration

Aeroplanes require the calculation of such values as altitude, speed and Mach factor from the air pressure in a pitot tube (fig. 3). A highly accurate AD conversion of the pressure signals received at the sensors is necessary for the processing of the data. The digitalised values are corrected by complex algorithms and then turned into air data. The use of a DSP to process the signals makes it possible to adjust the algorithms to a variety of sensors without changing the hardware.

The methodology that has been developed at IMMS has made possible the effective design of DSP-based mixed-signal ASICs. With the assistance of resource requirements estimation one can make sound decisions on the choice of a suitable processor. Simulating the system and the software models together enables testbenches to be produced conveniently without having to do without simulation of the system down to the last bit. The methodology has been demonstrated on the processing of pressure

signals in an air data system, with an ARC core.

Outlook

Future plans include improving the design methodology for DSP-based systems to such an extent that the non-electric environment may also be simulated (with VHDL-AMS, for example). An IP platform is planned, to enable the reuse and simulation of available blocks in addition to the processor. Practical application of the design flow to specific applications, such as a high-temperature sensor interface in SOI engineering is intended.

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Integrated Inductance

Objective

In the field of Radio Frequency (RF) circuit design, the work on planning, design and testing of integrated RF circuits is vital. This work will involve, in particular, transmitters, receivers and transceivers for applications using the license-free frequency bands, i.e. 433 MHz, 868 MHz, 2.4 GHz and 5.6 GHz. Oscillators used to produce the reference frequencies are of prime importance in these integrated circuits. LC oscillators give excellent performance but have rarely been used to date in low-cost applications. The main reasons have been the low quality level of integrated inductance's, and the difficulties they present for modelling. Now that integration technologies and their possibilities have progressed, as have CAD-tools for RF circuit design, the use of fully integrated LC oscillators is not only possible but is actually becoming sine qua non in view of the increasing complexity of these narrow band multi-channel systems.

Results

IMMS has been working intensively on the development and optimisation of integrated inductance. A variety of trial fields where designed and evaluated (see Fig.1). The inductor modeller contained in Cadence DF II is used to integrate them into the design flow. The design engineer can thus optimise the coil in the course of the design process, so that the circuit as a whole performs as efficiently as possible. Fixed coil layouts, the methodology used to date, which requires many iterations, are thus redundant.

Frequency [GHz]	Q_{max}	L_{min} [nH]	L_{max} [nH]
0,9	7,8	4	12
2,4	11,5	1,5	3,8

An overview of the parameters achievable for inductance integrated into a standard 0.6 µm BiCMOS technology, is given in the table.

The measurements on the coils were taken using an in-house RF measuring system: an HP 8510 network analyser. The S parameters of the coils were first measured and de-embedded using the accompanying open structure. It was then possible to extract the elements of the lumped electrical circuit model of the coil.

Fig. 2 shows the simulation results compared with measured results for one inductance as an example.

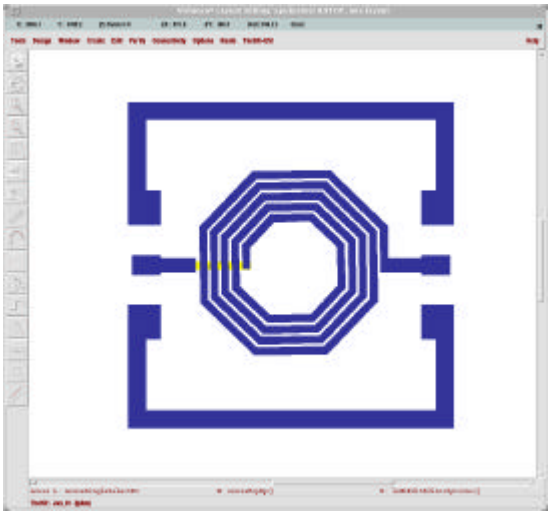

Fig. 1: Layout example of a integrated inductance

Outlook

Not only coils but a range of integrated varactors (of both the MOS and PN types) are under investigation at IMMS. The work on the characterisation of both, together with their modelling, is laying the foundations for the design of fully integrated LC-VCOs (Voltage Controlled Oscillators), which will replace ring oscillators in existing PLL (phase-locked loop) synthesisers. It will then be possible to realise fully integrated of RF circuits without expensive external LC tanks.

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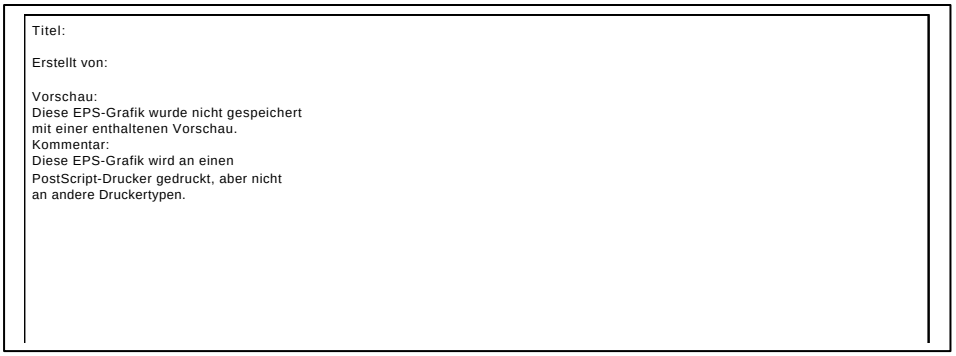

Fig. 2: Simulated and measured results compared, for a coil optimised to operate at 1 GHz (inductance and quality as functions of frequency)

The TH9353.1 Optical Line Sensor

Objective

Systems and components for automation and control systems are gaining ever more importance for manufacturing. The optical line sensor TH9353.1, which has been developed represents typical work on sensors and control systems on one hand, and on the computer-aided data processing to which they are connected on the other. The project has involved taking the design flow from start (creation of the specifications for the system) to finish (a fully designed and analysed ASIC). The way also led through deciding on which design method was efficient and developing new circuit elements. The project reached its goal in the course of 2001, with results which could be evaluated.

Progress and status of research

One significant result was the practical proof that the principle of functioning and measurement used by the optical line sensor was successful in use. The novelty in the sensor is the high resolution of the data obtained, combined with rapid processing. One potential application is holding the circuit against a barcode, which will then produce an equivalent field of light and shade. By means of 512 photodiodes, the field will be converted into matching analogue voltages which are then registered and sent for further processing as actual voltages capable of analysis. What happens is that the light-and-shade field becomes available to the analogue block outputs of the circuit as a multiple signal. There is an internal, separate, digital logic system regulating the data processing in such a way that the analogue block outputs can work on the next peripheral components, which are controlled by the processor. The line sensor is secured on a specially made glass carrier.

Outlook

Next year, some of the research will be concerned with developing further optotronic sensors. Another main emphasis will be on producing ASICs for optical data processing. The line sensor will be used in measuring systems of the future.

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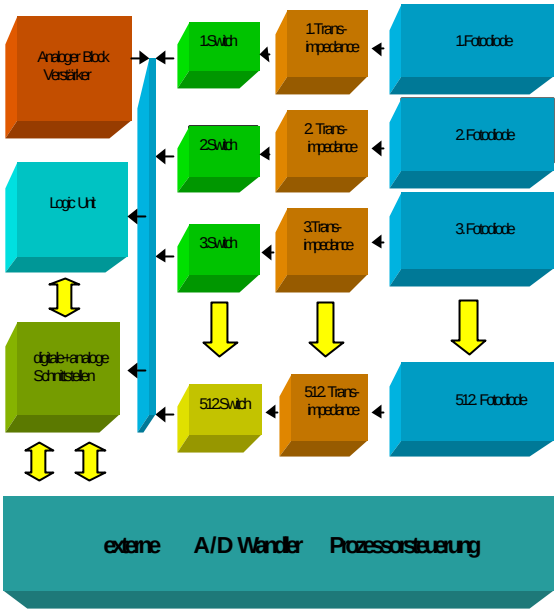

Fig. 1: Block circuit diagram of the TH9353.1 line sensor

	min	Typ	max
U_{DDA}	4.5 V	5 V	5.5 V
U_{DDD}	4.5 V	5 V	5.5 V
I_{DDA}		25 mA	
I_{DDD}		10 mA	
Clock		500 kHz	1 MHz
Z_{trans}	0.5 MΩ	1MΩ	1.5 MΩ
I_{Foto}	100 pA		200 nA
P_{out} **per analog channel**	18 dB	20 dB	22 dB
U_{out} **Hub per channel**	500 mV	1.8 V	2.2 V
Tem-peratur	-20°C	27°C	90°C
U_{ref}	2.2 V	2.5 V	2.8 V

Table 1: Specifications for the TH9353.1 optical line sensor

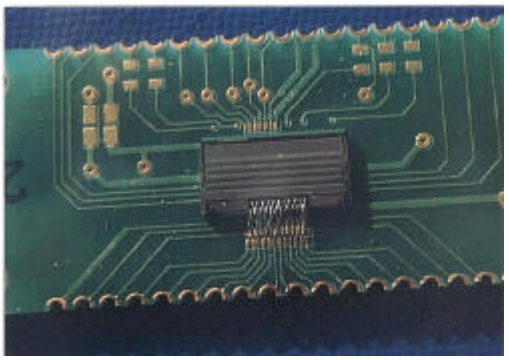

Fig. 2: The TH9353.1 line sensor as an ASIC

Integrated Optical Receivers for DVD Read- and Read-Write Devices

Objective

The DVD Blue project is researching the design of integrated optical receivers for the highly compressed representation of data. Such receivers are used in CD and DVD drives. The change from the infrared reading system used in CDs to red systems through focusing the light more sharply increased the degree of compression for the registration of the data significantly , in the case of CDs to 0.65GB, and in the case of DVDs to 4.7GB.

Progress and Status of Research

The work is at present concentrated on designing optical receivers for use in conventional DVD reading devices and in the DVD read-write devices of the future. The receiver circuit which has been designed for the purpose unites the photodiodes as sensor element, the linked TIA transimpedance amplifier and also the initial signal processing onto one and the same chip. The chip thus has four rapid reception channels which receive the focusing signal, a summative circuit for these channels so that the data signal (with frequency limit of 60MHz) can be emitted, and four slow receiving channels to produce the signal to set the position of the groove. The receiver for the DVD writer can work at the same speed in write mode as in read mode.

Outlook

Our aim will now be to increase the speed of normal DVD receivers and to develop the optical receivers for the next generation of DVDs. For these, blue laser light will be employed to enable the compression to be further improved, so that a single-layer, single-sided disk takes approximately 20GB. The reduced quantum efficiency of blue light does however mean that the photodiode supplies a smaller signal current with a higher frequency limit. The result is that the amplifiers then required must meet more challenging specifications in respective of bandwidth and sensitivity.

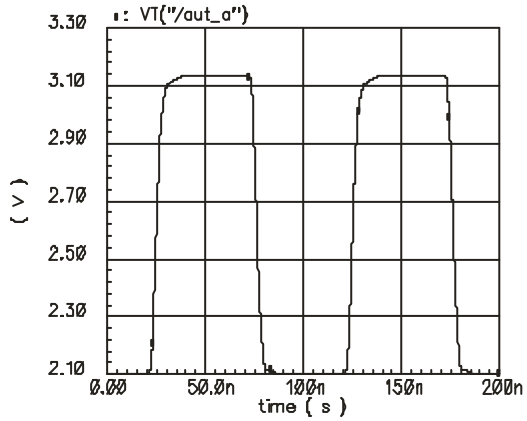

Fig. 2: Simulation results of a fast channel

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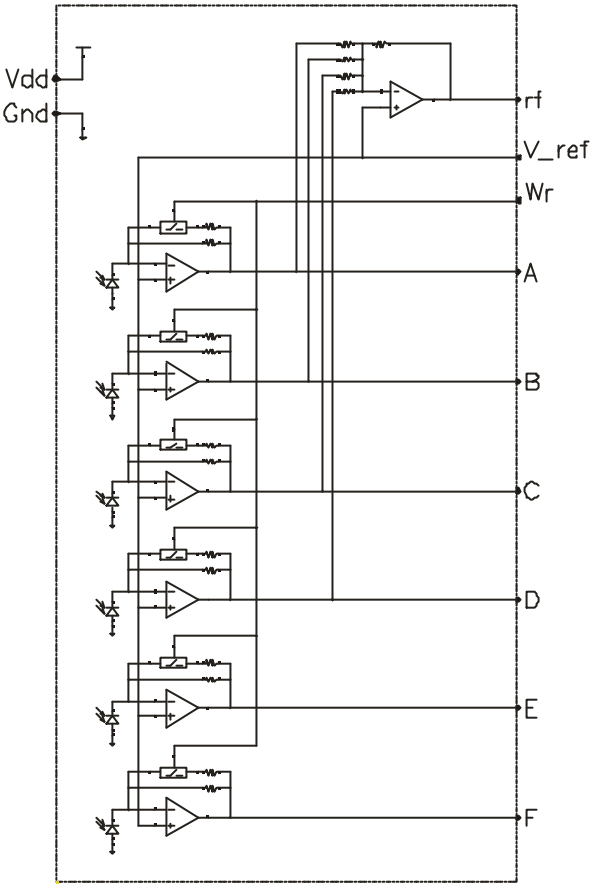

Fig. 1: Block circuit diagram for the DVD receiver

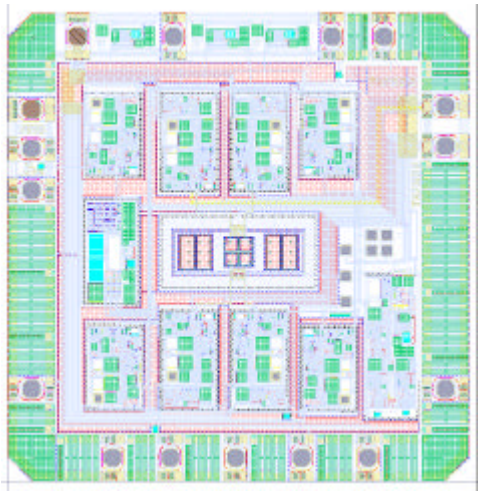

Fig. 3: Layout of the DVD read-write receiver

SOI Circuit Engineering
Q Device

Objective

As part of the project with the German name "Realisierung eines Qualifizierungs-Bauelements für die Digital-Library der X-FAB Technologie XI10", a Q-device chip was created, to assist in characterising the digital cells of the XI10 SOI technology from X-FAB:

- Validation: logical function, timing, power consumption
- AC/DC parameter test
- ESD test
- IDDQ test
- Test of reliability/lifetest
- Failure investigation
- Design kit/flow Verification.

Progress and status of research

The position as at September 2001 from the X-FAB project "Digital Cell_Q_Device" was taken over and used as the basis for concrete implementation with digital cells of the XI10 technology.
The original device consists of two parts: a combinatorial with inverter, buffer, tristate (N)AND, (N)OR, EX(N)OR, and FA, and a sequential with flip-flops and latches. The first, combinatory, part of the plan was put into practice initially.
The testing scheme for the XC06 process was modified to match the XI10 technology. The volume was reduced to match the current number of gatter on the XI10, and the schematics were simplified. So as not to spoil the general applicability of the scheme, i.e. its ease of transfer to any X-FAB technology, dummy structures were put in where gatter and blocks of lattices were missing. By doing this, the developers enabled the Q-device to be tested in future with universal pattern sets.
The combinatory part consists in 10 blocks which are comprised of sub-blocks with a varying number of individual gatters. These sub-blocks contain the single gatter for testing the logical function, and a chain of gatters for measuring such dynamic characteristic data as delay times and rising and falling edges. The chains may be driven open or as a ring oscillator, and are tested under both continuous and pulsed operation mode. The device also offers the possibility of testing the input-output cells of the XI10 technology using a NAND tree. The layout of the Q-device is shown in fig. 1.

Outlook

Completion of the Q-device chip is planned for March 2002 and will be followed by measurement of its characteristics. These measurements will be taken using the test pattern sets which have already been generated.

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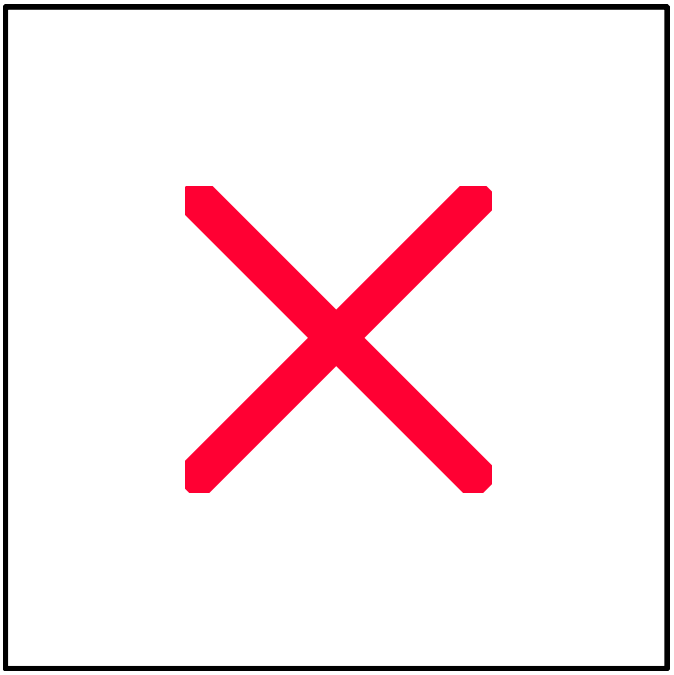

Fig.1: Q-Device layout

SOI Circuit Engineering
Memory Development

Objective

The SOI section is working on circuits for sensor interfaces as an internal project. One interface has already been developed and now work is proceeding on a memory for it (based on SRAM and EEPROM), capable of being written over to permit data to be stored so that the characteristic curves of the measurement readings can be corrected. The block diagram for the sensor interface is shown in fig. 1 at the planning stage.

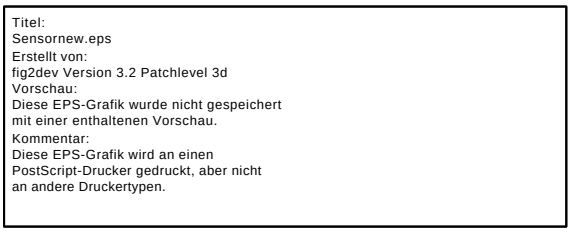

Fig.1: Block diagram of a sensor interface

Progress and status of research

October 2000 saw the commencement of the SRAM memory development work at IMMS, with the devotion of a 'Diplom" dissertation to the matter. The work has produced a 256x8 bit memory with all the peripherals: sense amplifier, bit line pre-charge and decoder. When measurements had been taken, the memory was adjusted, expanded and matched to the changes which had meanwhile taken place in the SOI technology. Fig. 2 shows the layout of the second generation SRAM memory chip. The block of memory cells and the position of the main peripherals are indicated.
An array of 256x32 SRAM double cells, where each cell stores 2 bits, is at the core of the memory. Word line and bit line decoders allow access to the desired 16-bit "data word". The word line decoder is an NAND decoder divided between both sides of the array of cells. The bit line decoder is simply a version of a 2:1 multiplexer. Both the address path and the data path contain drivers to maintain levels. The reading circuits marked "2" in the illustration permit the data to be read without their being destroyed. The signals required for read or write are provided by the controller. The memory is contactable from outside via data lines and address lines, and also by a signal for reversing direction. The controller also requires a clock signal.
As the EEPROM design process requires modification, the SRAM development has a year's start on the alternative. So far, various types of EEPROM and EPROM individual cell have been designed. In addition, some of the peripheral elements for the intended non-volatile memory, the high-voltage switches and charge pumps, have been simulated and created as individual trial structures.

Outlook

Measurements taken on the test structures will help identify suitable layouts and indicate where re-design would be of benefit. When the SRAM has been subjected to measurement it will also undergo the re-design process. The SRAM will also be provided with a built-in self-test device. The goal of the memory development work is that the SRAM and EEPROM should not only be installed in the currently projected sensor circuit but should also be generally available within the design kit.

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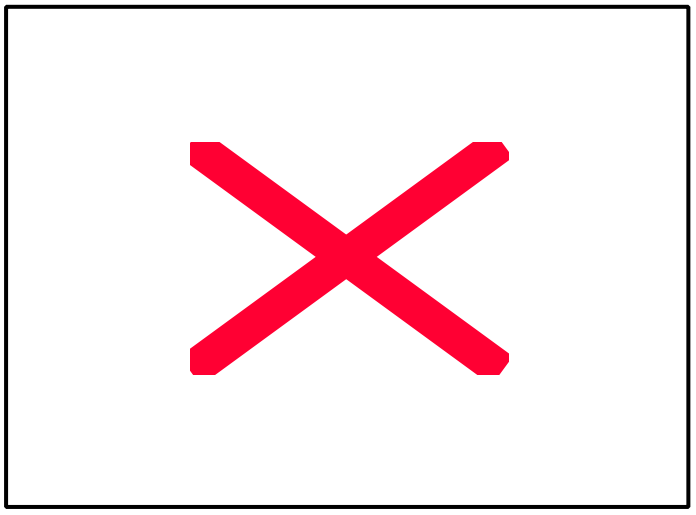

Fig. 2: Layout of the 1Kx16 bit memory circuit

SOI Circuit Engineering
Design Kit

Objective

X-FAB Semiconductor Foundries AG commissioned IMMS gGmbH with a project which included the production of a design kit for the X-FAB XI10 technology, which is based on a 1.0 µm SOI CMOS process. The industrial partner bore the responsibility for the design support. IMMS gGmbH undertook to provide maintenance such as the incorporation of novel or modified elements. The project was completed in 2001.

Progress and status of research

The design environment used for the design kit was Cadence Affirma Spectre mixed-signal design. This package is a development environment of value to the designers of mixed-signal systems and layouts. There is little basic difference between the design flow (shown in fig. 1), supported by the design kit, and that for a standard CMOS process.
The flow starts with the schematic entry of digital or analogue circuits. The next thing is the

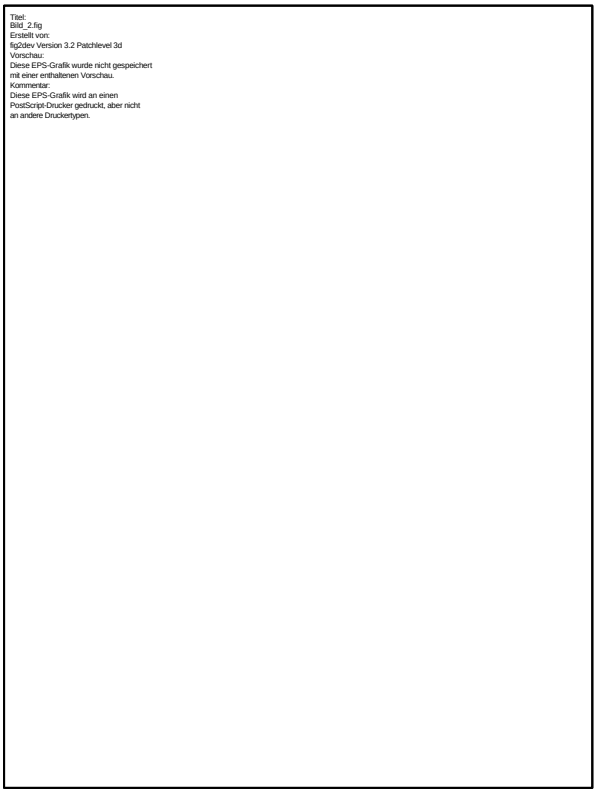

Fig. 1: Representation of the design flow

pre-layout simulation. Layout follows. Post-layout simulation, which produces data in GDSII format for the wafer manufacturer, is the last stage. The behaviour which requires most attention for analogue circuits when SOI is being used is taken account of by the models in the design kit. Examples of this behaviour are the kink effect, self-heating of transistors or back-side contact with the substrate. There is also an MPW service for the X-FAB process, which is also available to smaller companies.
The design kit includes a standard cell library of digital cells, a library with input and output cells, such primitive elements as transistors, diodes, resistors, linear capacities, a variety of high-voltage transistors (for 30, 60 and 90 V) and a Hall element to detect magnetic fields. It can also optionally contain a linear capacity and a with high impedance poly resistor. No special masks are necessary for the Hall element (see fig. 2) as it is possible to use the n-drift range of a high-voltage transistor to create a Hall plate. The reason is that the Hall voltage generated by a magnetic field is in reverse proportion to the thickness of the active silicon layer (tSi=250nm). Further implants are usually necessary in standard processes to produce the thickness of Hall plate surfaces. It is in the primitive elements that most deviation is to be found from the standard bulk CMOS technology. Designers familiar with such standard systems are easily enabled to create their own layouts with the help of PCELLs, which are 'parametrisable" cells, for each primitive element. The fully synthesisable standard cell library for the digital cells is available in two versions: one for Cell-Ensemble wiring and one for Silicon-Ensemble. The I/O library includes input, output and bi-directional cells with a variety of driver power and in either open-drain or open-source versions. There are also power cells for the electricity supply, and filler and corner cells to complete the ring. The requirements for mixed-signal layouts are thus fulfilled.
To protect the design against incorrect entries, there is a checking system included in the design kit for circuit verification. The design rule check will make sure that the layout rules currently valid are in conformity with the primitive elements and with the overall physical layout. By extracting the layout it is one possible to gain information on parasitic components included in the layout. This process also produces a list for the layout-versus-schematic (LVS) check. The layout extraction process distinguishes between simple extraction and extraction including parasitic elements.
The elements seen as parasitics are capacities existing between wires, to the substrate, and resistors within wires. The two options can be selected independently of one another, and it is possible to distinguish in the extraction which

includes parasitic elements between extracting capacities and extracting resistors.

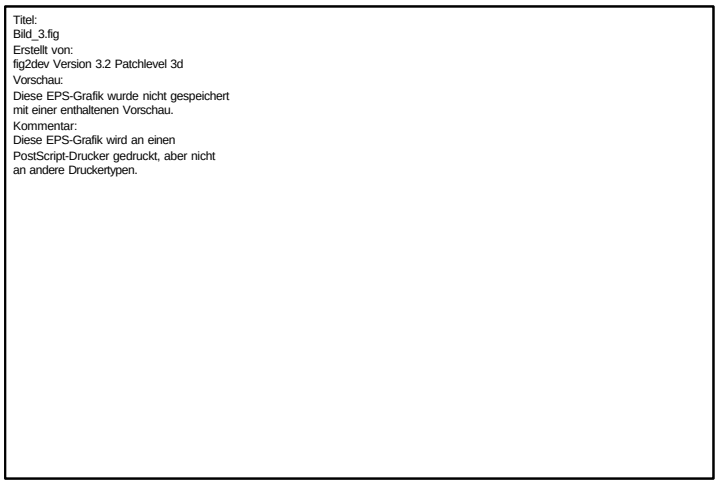

Fig. 2: SOI-Hall element

tion. Spectre or Hspice (made by Avant!), which are available under Analog Artist, will permit analogue simulation of the circuits.
Models and sets of parameters are included in the design kit for both these circuit simulators. Bulk MOSFET models (BSIM3v3) and models specific to SOI (BSIM3SOIPD) are available as transistor models, with the relevant sets of parameters. There are sets of model parameters for resistors, capacities and diodes (where the length of one diode is equal to the thickness of the silicon layer).
The timing data required for digital simulation using Verilog are also included. Analog Artist is the tool used for mixed-signal simulation. There is no difference between this design flow and a standard design flow. The main differences are in the transistor models and in the layout of the primitive elements. These are not modified by the user of the design kit.

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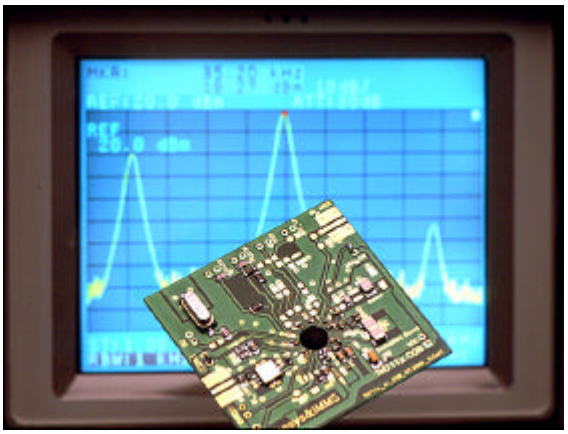
The LVS checks whether the layout deviates from the schematic previously entered, and is also the prerequisite for the post-layout simula-

Analysis and Testing

The Department of Analysis and Testing offers measurement and analysis systems for use in support of industrial research projects as well as to accompany research and development work within IMMS. The emphasis is on:

- High frequency measurement technology to determine S parameters up to 50 GHz
- Determining noise parameters in the frequency range from 300kHz to 26GHz
- Testing ASICs in digital or mixed signal mode
- Measurement technology used to characterise AD/DA converters.
- Standard measuring technology for the



characterisation of digital/analogue circuits

2001 saw the fruits of many years of experience in high frequency component characterisation, firstly in successful designs for high frequency applications, and secondly in tailor-made solutions to measurement problems. Market-leaders in chip manufacture now number among our clients. IMMS has also been able to demonstrate its skills at national and international conferences and has been accorded much recognition for its research.

In order to manage the expected rise in workload in the field of ASIC testing, the number of staff has been increased in this Department. The idea is that experience gained in the test work so far done can be put to good use in the designing of ASICs. In addition, measurement technology is continuously expanding as hardware and software components are introduced with the aim of making the test runs more automatic.

The measurement capabilities in this department have been expanded by components that make both static and dynamic characterisation of AD/DA converters possible. Know-how which has already been integrated into ongoing projects has thus been collected. The objective, measurement technology with a 14-bit resolution that has been tested and is ready for use, will be met in the course of 2002. That will make it possible for IMMS in the following years to bring high performance testing and measurement technology to bear on their design of AD/DA converters.

The Department will work on circuit design in addition to the previously mentioned testing and measurement tasks. The foci will in this case be HF circuit technology (GPS/GSM applications) and power electronics (electronic ballasts for fluorescent lamps).

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Characterisation Procedures for Fuses using 0,6 µm Technologies, and Optimising the Programming

Objective

Semiconductor circuit engineering is today unimaginable without OTPs (which can be programmed only once). Fuses are one representative of these primitive devices. They are what they say, a means of keeping a circuit balanced at the wafer level. With this type of fuse and the right electronic analyser, it is possible to meet higher accuracy specifications for analogue circuit segments without specialised equipment. The programming can change the fuse resistance from a few hundred ohms to the range in the thousands. These flexible fuses can be used, for instance, in automotive or general communications systems.

They are an element of design kits for semiconductor foundries. This particular project involved research on behalf of such a company, X-FAB of Erfurt, to discover optimum programming conditions and to produce measurements for characterisation. The results will be used in the design kits being created for X-FAB's XB06 and CX06 systems.

The following aspects are of particular interest:

- *Programming*
  Voltage, current and time conditions under which the fuses may be safely programmed with manufacturing equipment must be set.
- *Reversible area*
  The voltage range of the fuse programmed in the reversible area is selected in such a way that the analysing circuit recognises it as programmed. Return to the unprogrammed state takes place without any alteration to the fuse characteristics. The reversible area is important for production testing, so that the best fuse to balance a circuit can be selected.
- *Reliability*
  Statements on reliability and long-term stability must also be made. Here, what is crucial is the influence of different programming features on reliability. Q devices are used during life testing to determine reliability.

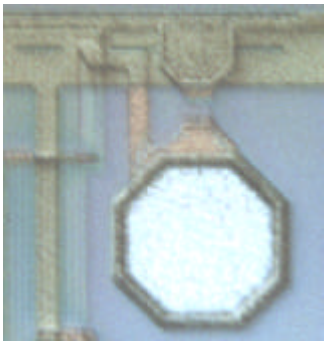

Fig. 1: Chip photograph of a fuse

Progress and status of research

Carrying out the set task in real life required that the developers knew exactly and with statistical certainty how the fuse would behave in the course of programming. For the purpose of this characterisation, a measurement system was designed and constructed. It was based on the HP82000 IC evaluation test system with certain external components and gauges for the sake of exact investigation. It was, namely, essential to determine the features of the fuses as precisely as possible. Kelvin wire guides were used for the analogue section. Comparisons between various sets of equipment were also carried out. The software for testing was implemented in HP-VEE.

At this stage, it was important to have the facilities for close analysis and visualisation of the readings from the various series of measurements, with particular emphasis on:

- *c / v characteristic curves*
  These were plotted for various step-widths and times. Variation between the v force and c force programming modes.
- *c / t characteristic curves*
  Analysis of what happens in real-time in the course of programming. Measuring kit including oscilloscope and metal clips for current.
- *Measurements of R*
  Exact measurement of the fuse resistance before, after and in the course of programming.
- *Reversible area*
  The extent of this area was determined using a specialised testing program. It had the aim of determining the maximum voltage produced by no long-term alteration of the resistance at the fuse.
- *Digital testing*
  The fuses are integrated onto the chip with their electronic evaluation circuits. This means that programming success can be measured digitally. Multiplexers permit the evaluation circuits on the fuses (up to a total of 64) on the chip to be contacted.

After a range of technical solutions and layouts had been investigated, the best programming pattern for each individual type of fuse was deduced.

The project also involved transferring the programming conditions as obtained into a measurement system appropriate to production, without any additional equipment and without possibility of analysis. The measuring system is to enable fuses to be programmed onto test

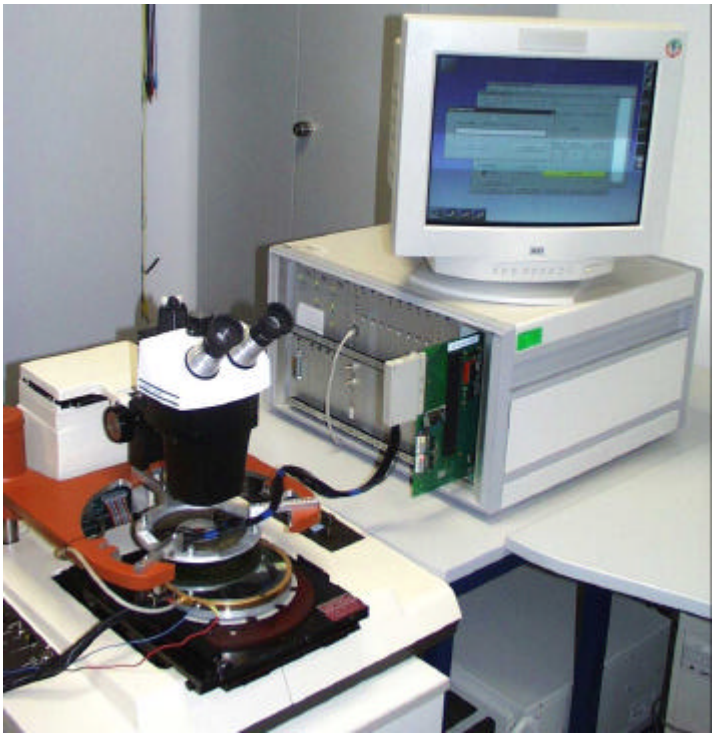

Fig. 2: Taking wafer measurements with the Sigma Delta

chips which, when built up into Q devices, will provide the basis for investigations of reliability. For that reason, a measuring system for production purposes was designed which would work with the Sigma Delta test system. The hardware used for the testing includes wafer measurement, programming of the fuses and device measurement on the chips in their housing. C was used to implement the individual testing and checking programmes. The research included developing the loadboard for the testing system from start to finish.

The programming conditions for the Q devices were established, so that it was possible to make statements on reliability for a number of different programming regimes. The criteria on which the conditions were selected tended to be what had been learnt from the characterisation, or which best covered the relevant current and voltage range, or whether ordinary, conventionally manufactured test equipment could be applied under them.

All measuring and programming of the chips for the Q-devices took place in house at IMMS. The measuring equipment for the production stage was made available to the commissioning partner to take interim measurements during life testing, and transferred to Erfurt.

Outlook

The project ran from September to December 2001, in association with X-FAB Semiconductor Foundries AG's Design Department in Erfurt. The life test will be concluded during the first quarter of 2002.

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PCBoard Layout: High Frequency - High Speed

Objective

The performance of a printed circuit board (PCB) is determined on the one hand by the design of the circuit and on the other by the layout that proves possible on the board. The importance of layout applies particularly to the analogue and RF design. However, even in the digital circuit engineering task, which can easily involve switching frequencies of 100 MHz and pulse edges below 1 ns, it is no longer possible to look on the paths for the circuit tracks on a board as automatically ideal links.
Only with thoughtful development of the board is the target of a minimum number of iterations in expressing the original idea as a fully functional product to be achieved.

Status of Research

The development of the board itself is a major step within the design flow. A circuit which is functional at the schematic level is not bound to turn out as a properly functional circuit on the finished board. Simulations tend not to pay sufficient attention to a number of parameters which have a strong influence on function.
The following factors, in particular, are liable to have a negative effect on circuit functioning:

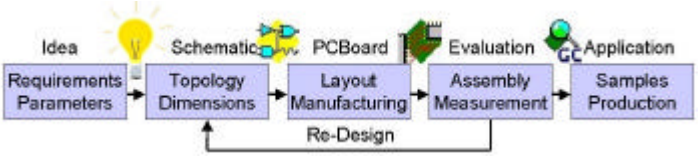

Fig. 1: Basic steps in development of a board

- Stray coupling or crosstalk between circuit paths
- Attenuation, reflection and transit time on the paths
- Parasitic capacitors and inductors processed by wiring and components
- Leads for ground connection or operating supply which are unfavourable.

The negative effects may be oscillations, poor selection or low sensitivity, distorted pulses or interference from irregular, intrusive pulses. How the board is laid out will also determine how much radiation of electromagnetic waves takes place, or the degree of sensitivity to incoming radiation. Suppression of radio and electromagnetic interference is required to achieve CE conformity and can only be achieved if the PCB is thoughtfully designed.
Specific layout problems have been investigated in a variety of projects with industrial partners. At the same time as enabling the designers to derive rules for design methodology and for the marginal engineering factors and other limitations, the work has led to practical solutions and proven components.
The applications successfully produced included:

- A passive high speed backplane for data transfer rates of up to 2.5 Gbit/s (for ADVA, Meiningen)
- Evaluation boards for HF-ICs, e.g. a single chip receiver (for Melexis, Erfurt)
- Components for GPS and GSM applications (for Falcom, Langewiesen)
- Testcards and testing equipment for IC testers (for XFab, Erfurt)

Connections with controlled impedance

It is absolutely essential that circuit boards for high-frequency applications and/or high data transfer speeds are designed to include impedance control of the wiring on the platen. **Microstrip** or **stripline** structures are appropriate. They can take a single-ended or differential form. The size they are given will depend on the following factors:

- the width of the wiring
- the thickness of the copper
- the dielectric coefficient ε_r of the material used as substrate
- the thickness of the substrate down to the next grounded layer

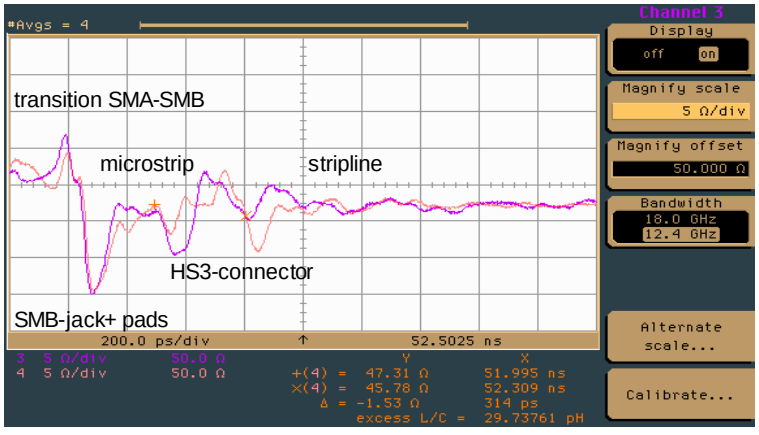

Fig. 2: TDR measurements taken on a passive backplane

If Microstrip lines are used, the soldering mask, also, has an influence on the RF parameters which cannot be disregarded. All measurements and values must be known and, where appropriate, passed on to the PCB manufacturer as exact figures.
The components and materials used (radio and electromagnetic interference suppressers, plug-in connectors, platen materials and so on) must all be strictly suitable for the use intended and the frequency range required in the particular case. Technical data sheets should specifically document this suit-

ability. Where structures are very narrow (< 0,2 mm), the tolerances require close analysis. Not even the most careful construction will achieve tolerances lower than 5 %.
In this year's work, trial structures were designed for the evaluation and verification of impedance-controlled layouts on FR4 materials, and then measurements taken. The impedance along a plug-in card on a backplane was measured at various points using a time domain reflectometer (TDR). The individual sections of the wiring and the transitions are to be clearly seen in fig. 2.

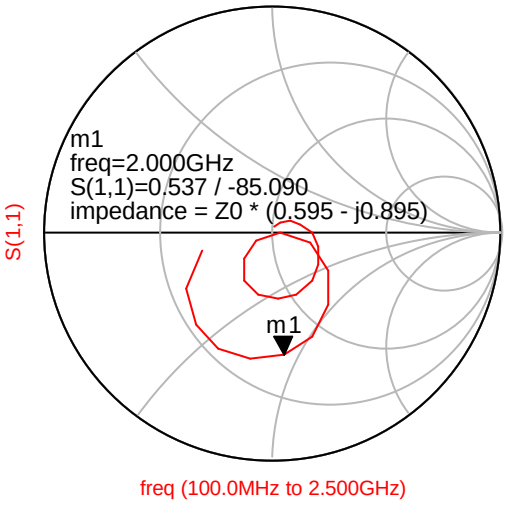

Fig. 3: Transformation of impedance on a line

The software used to set and simulate wiring sizes was the Agilent package (ADS). On a wire with deviation in wave resistance of 10 ohms and connected by plugs, the change in impedance is represented in fig. 3 by means of the frequency. Particularly in the case of the high-frequencies which reflect the steep pulse edges of a digital signal, complex impedance figures deviating widely from 50 ohms are found.

Assembly technology

The fitting and assembly possibilities for RF applications include not only the usual SMD but also, and with particular suitability, chips bonded onto the board (COB). This method saves space and reduces the parasitics, as it involves shorter bonding wires, no housing, and smaller pads on the board. A trial board was built on these lines so that it could be evaluated for the 868 MHz superhet receiver (TH7111). The basic material used for the PCB was FR4, 1 mm thick, and the narrowest structure was 0,2 mm, which reflects standard manufacture.
The circuit paths require surfacing with bondable gold.
By this means, the surface of the PCB is reduced to less than half the size achieved with conventional SMD packages.
No significant differences were found in respect of RF performance using this technology. Whatever the layout, it is important to minimise the resistance of the ground contacts of the individual circuit components.

Services

IMMS can provide services in the following fields:

- Circuit design
- Design of PCBs
- Construction of trial boards / systems
- Descriptive analysis using measurement of DC and HF up to 50 GHz
- Consultancy and training

The engineers at IMMS have not only a wide variety of design and measurement tools available to assist their industrial partners, but also the necessary know-how and experience.

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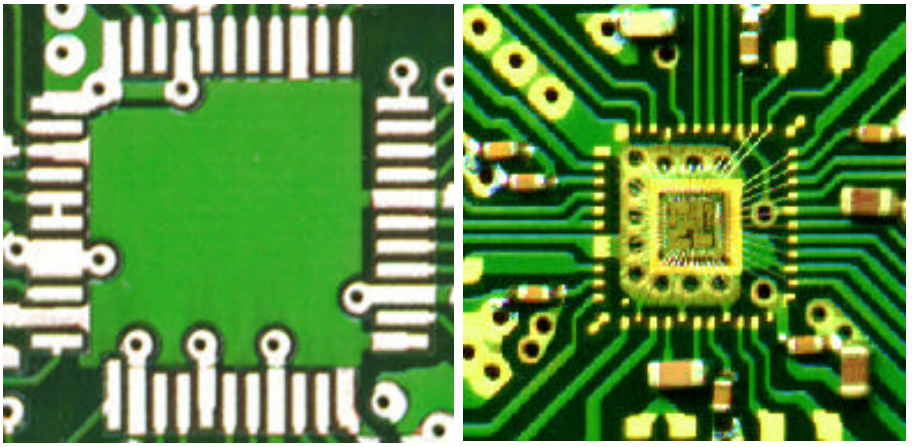

Fig. 4:
Sizes of chip on board (COB) and SMD layout compared for TH7111. 44 pins, size of section in each case 13x13 mm.
The photograph on the right shows capacitors of the package 0402 (1 x 0.5 mm) and 0603 (1.5 x 0.75 mm) on the COB board.

Membership of Professional Associations and Working Parties

- **Mitglied Leitungsgremium der GI/GMM/ITG-Kooperationsgemeinschaft "Rechnergestützter Schaltungs- und Systementwurf (RSS)"** (Fachausschuß 3.5 der GI, Fachbereich 8 der GMM, Fachausschuß 5.2 der ITG)
- **GI/GMM/ITG-Kooperationsgemeinschaft "Rechnergestützter Schaltungs- und Systementwurf (RSS)"** Fachgruppe 1 "Allgemeine Methodik und Unterstützung von Entwurfsprozessen für Schaltungen und Systeme"; Fachgruppe 2 "Entwurf von analogen Schaltungen"
- **GMM -** Beirat
- **DFAM -** *Deutsche Forschungsgesellschaft für die Anwendung der Mikroelektronik e.V.*
- **VDE / VDI Fachgesellschaften ITG, EKV und GMM**
- **VDE / VDI - Arbeitskreis Mikrotechnik Thüringen**
- **Facharbeitsgruppe Mikrotechnik Thueringen (TMWAI-STIFT)**
- **Steuergremium des EDAcentrums**
- **ITG-Arbeitskreis "Zusammenarbeit Industrie und Hochschulen"**
- **ITG Fachgruppe "CAD für den Analogschaltentwurf"**
- **IEEE -** Circuit and Systems Society; Electron Devices Society; Solid-State Circuits Society
- **EIBA -** *EUROPEAN INSTALLATION BUS ASSOCIATION*
- **VSIA -** *VITAL SOCKET INTERFACE ALLIANCE*
- **USB - Implementer Forum**
- **MSDN -** *MICROSOFT DEVELOPERS NETWORK*
- **VDMA - Arbeitskreis "Nutzergruppe Mikrosystemtechnik" im VDMA**
- **TZM Erfurt -** *Technologie-Zentrum-Mikroelektronik e.V.*
- **InnoRegio Südthüringen e.V.**
- **MTT Mikrotechnik Thüringen e.V.**
- **Industriegebiet Erfurt Südost e.V.**
- **GNT -** *Gesellschaft zur Förderung neuer Technologien Thüringen e.V*
- **OptoNet e.V. Thüringen**
- **AZT e.V.** - *Automobilezulieferer Thüringen e.V.*
- **Fraunhofer Gesellschaft / IOF Jena**
- **EUROPRACTICE**
- **American Chamber of Commerce**
- **DFN**
- **Programmkomitee Technologiesymposium MTT 2002** (Mikrotechnik Thüringen)
- **Member of the Review Board of the TELSIKS 2001** (5th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services)
- **Mitglied des „Inneren Arbeitskreises“ FUTUR des BMBF**
- **Jury des BMWi zum Initiativprogramm “Zukunftstechnologien für kleine und mittlere Unternehmen”** - ZUTECH 1999 – 31.7.2003
- **Programmkomitee GI/GMM/ITG Fachtagung "Entwurf Integrierter Schaltungen" E.I.S.-Workshop, 2001**
- **Programmkomitee/Reviewer DATE 2001**
- **Strukturkommission für die Hauptabteilung Prozessdatenverarbeitung und Elektronik (HPE) 2001**

Papers and Publications

- **“Erfahrungen mit der UML beim Entwurf von Kfz-Steuerungen”**

M. Götze, W. Kattanek, (IMMS gGmbH)
ITG/GI/GMM Workshop "Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen", 02/2001, Meißen (Workshop contribution on circuit and system modelling and verification)

- **Systems on Chip: “Übersicht zur Simulation von "Multi-Nature" – Systemen”**

Prof. F. Rößler (IMMS gGmbH)
Regionalgruppe Ilmenau der Gesellschaft für Informatik, Ilmenau, 02/2001 (Local workshop for Informatics Society)

- **“DSP-Software Entwicklung aus Simulink Modellen / C-basierter Hardwareentwurf mit den AIRT Tools von Frontier Design”**

C. Lang (IMMS gGmbH)
DFAM AK-Sitzung, 02/2001 (Meeting of DFAM [German Research Assoc. for Application of Microelectronics] working party)

- **“Experiences with the UML in the Design of Automotive ECU”**

M. Götze, W. Kattanek (IMMS gGmbH)
“Design, Automation and Test in Europe” (DATE) 2001, München03/2001 (International Conference)

- **“DSP-mixed-signal-ASICs”**

Prof. F. Rößler, C. Lang (IMMS gGmbH)
DFAM Beiratssitzung, Freiburg, 03/2001 (Meeting of advisory council to DFAM)

- **“Entwurfsmethodik für DSP-basierte mixed-signal-ASICs”**

C. Lang (IMMS gGmbH)
CeBIT 2001, Hannover 03/2001 (International Trade Fair)

- **“Kick-off-Meeting zum Projekt "ASDESE"”**

Prof. F. Rößler. (IMMS gGmbH), C. Foss (Melexis)
Reutlingen, 03/2001 (Start of the ASDESE project)

- **“Kick-off-Meeting zum Projekt "ANASTASIA"”**

R. Izak, S. Lange, Prof. F. Rößler. (IMMS gGmbH)
München, 03/2001 (Start of the ANASTASIA project)

- **“DSP und Mixed-Signal-ASICs”**

C. Lang (IMMS gGmbH)
8. Sitzung des Wissenschaftlichen Beirats des IMMS, Ilmenau, 03/2001 (8th meeting of the scientific advisory council to IMMS)

- **“Abschlußbericht zum Förderprojekt LPKM”**

M. Lange (IMMS gGmbH),
Ilmenau, 03/2001 (Concluding report on the LPKM* project)

- **“Top-Down Entwurf eines zyklischen A/D-Wandlers unter Einbeziehung der Verhaltensmodellierung in Spectre HDL”**

R. Izak, R. Kindt, Prof. F. Rößler (IMMS gGmbH), J. Stroemer (Melexis)
10. EIS-Workshop "Entwurf Integrierter Systeme", Dresden, 04/2001 (10th workshop on "Design of Integrated Systems")

- **“Modellbasierter Entwurf von DSP Systemen basierten mixed-signal Systemen in Sensorsignalverarbeitung”**

C. Lang (IMMS gGmbH)
IHP, Frankfurt/Oder, 04/2001 (International Conference)

- **“Entwurf eines digitalen Dezimationsfilters für einen 16-Bit Sigma-Delta-Modulator”**

U. Möllmann (IMMS gGmbH)
IMMS u. TU Ilmenau, Diplomarbeit, 04/2001 (Dissertation for the Diplom [equivalent of Master's])

- **“Entwurf eines digitalen Dezimalfilters in MATLAB”**

O. Richter
Praktikumsbericht IMMS Ilmenau, FH Zittau, 04/2001 (Report after practical placement at IMMS)

- **“Design of Silicon High Temperature Circuits - Entwurf von Silizium Hochtemperatur-Schaltungen”**

Dr. D. Nuernberg (IMMS gGmbH)
Ilmenau 05/2001

- **“Kick-off-Meeting ASEDA Projekt VALSE”**

C. Lang (IMMS gGmbH)
München, 05/2001 (Start of VALSE project for ASEDA)

- **“Entwurf von HT-Schaltungen mit einer 1.0µm SOI Technologie”**

Dr. D. Nuernberg (IMMS gGmbH)
München, SOI-Workshop, 05/2001 (Workshop)

- **“Decomposition of Multi-Valued Functions into Min- and Max-Gates”**

C. Lang (IMMS gGmbH)
Warsaw, 05/2001

- **“31st IEEE Symposium on Multiple-Valued Logic”**

S. Richter (IMMS gGmbH)
pp. 173-178 SOI-Technologien der XFAB München, 05/2001(contribution to company brochure)

- **“Design of Silicon High Temperature Circuits - Entwurf von Silizium HochtemperaturSchaltungen”**

GMM-Workshop
SOI-Workshop Nuernberg, 05/2001

- **“Bugreport Problems of SOI Models in Spectre”**

H. Liebing, Dr. Nuernberg (IMMS gGmbH)
Ilmenau (Ver.4.4.5.100.55 -28. Feb.2001), 06/2001

- **“Meeting ASEDA Projekt ANASTASIA - WP2”**

R. Kindt (IMMS gGmbH)
Meylan 06/2001

- **“Meeting ASEDA Projekt - ANASTASIA - WP3.1”**

S. Lange (IMMS gGmbH)
München, 07/2001

- **“A cyclic RSD analog-digital converter for embedded applications”**

R. Izak, J. Stroemer, R. Kindt (IMMS gGmbH)
Bratislava, Slovakia, Proceedings of 3rd ECS´01, pp. 97-100, 09/2001

- **“Möglichkeiten und Grenzen der Softwaregenerierung für den ARC Core / Software eines Luftdatenrechners auf dem ARC Core”**

C. Lang . (IMMS gGmbH)
DFAM-Sitzung 09/2001 (Meeting of DFAM)

- **“eCOS - Ein Open-Source-Betriebssystem für den Einsatz in komplexen eingebetteten Systemen”**

Dr. A. Schreiber (IMMS gGmbH)
IMMS F&E Report, Ilmenau, 10/2001 (R & D report)

- **“Hardware-Design mit SystemC”**

J. Zellmann (IMMS gGmbH)
Ilmenau, IMMS F&E Report, 10/2001 (R & D report)

- **“Rauschmessungen für die Kommunikationstechnik”**

B. Bieske (IMMS gGmbH)
Kamp-Lintfort, BRD, ITG 9.1 Diskussionssitzung, 10/2001 (Discussion at ITG)

- **“Die Herausforderung evolutionärer Systeme”**

H. Sankowski (IMMS gGmbH)
Ilmenau, IMMS F & E Report, 10/2001 (R & D report)

- **“Low Power Funkmodul für das 868 MHz Band”**

B. Bieske (IMMS gGmbH)
Entwicklerforum Low Power Design, München, 11/2001 (Developers' Forum)

- **“6th Status Seminar on Optical Data Storage”**

S. Lange (IMMS gGmbH)
2001 EUREKA blueSPOT , Villingen 11/2001

- **“Die Technische Universität Ilmenau - ein traditioneller Partner für Forschung und Entwicklung in Ostbrandenburg”**

Prof. G. Scarbata (IMMS gGmbH)
IHP Frankfurt/O., Workshop Kooperation Hochschule-Unternehmen, 12/2001 (Workshop on joint work by universities and industry)

- **“Linux-basierter universeller Buskonverter für die Automatisierung”**

J. Pietrusky, R. Peukert, Dr. C. Schröder. (IMMS gGmbH)
Fachzeitschrift "Electronic Embedded Systems", 11-12/2001 (Scientific journal)

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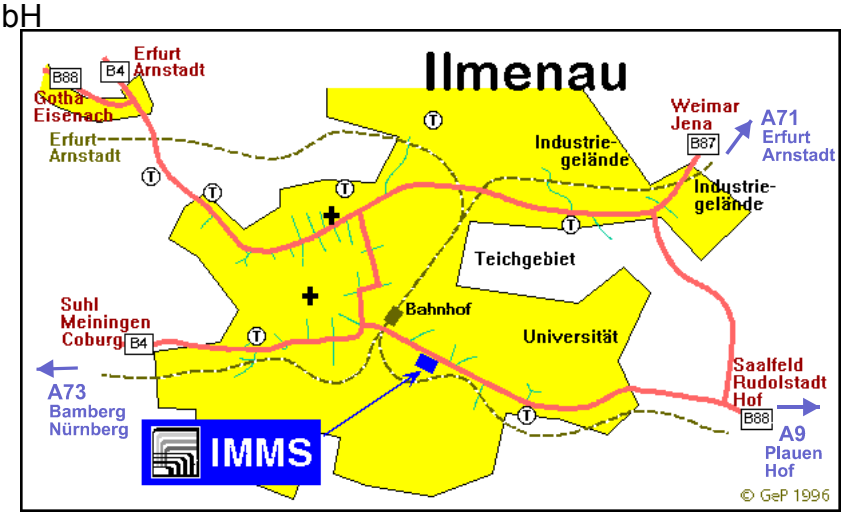

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